

GA-MA770T-UD3P

Revision : 1.1

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A vertical bar is divided into four segments labeled A, B, C, and D from bottom to top. An arrow points to the boundary between segments B and C.

A vertical bar with a horizontal arrow pointing to the right. The label 'B' is positioned below the arrow, and the label 'C' is positioned above the arrow.

01

A

[illegible]

1

A vertical number line with four points labeled A, B, C, and D from bottom to top. An arrow points to point C.

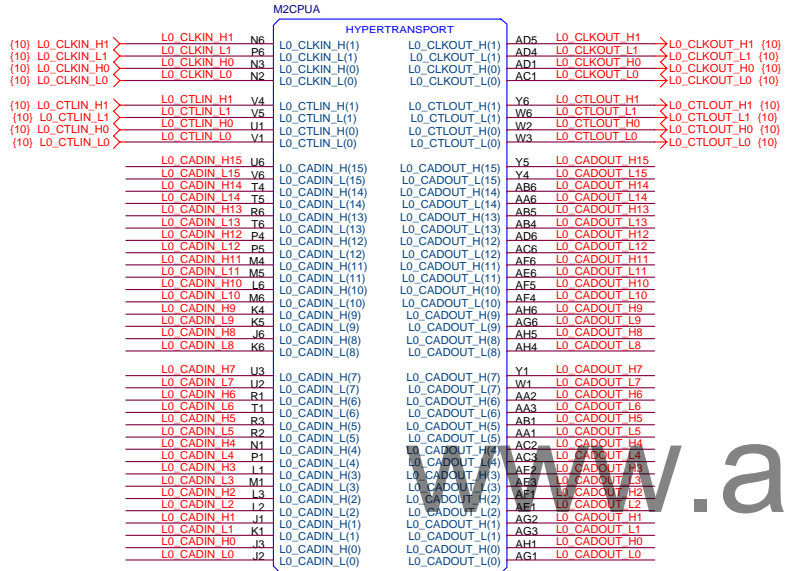
A

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L0_CADIN_L[0..15] <L0_CADIN_L[0..15] (10)
L0_CADIN_H[0..15] <L0_CADIN_H[0..15] (10)
L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] (10)
L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] (10)

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12

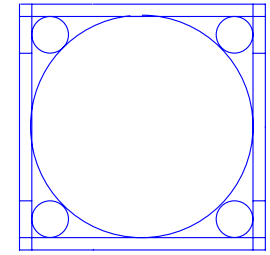
VLDT_A = VCC12_HT
VLDT_B = HT12B



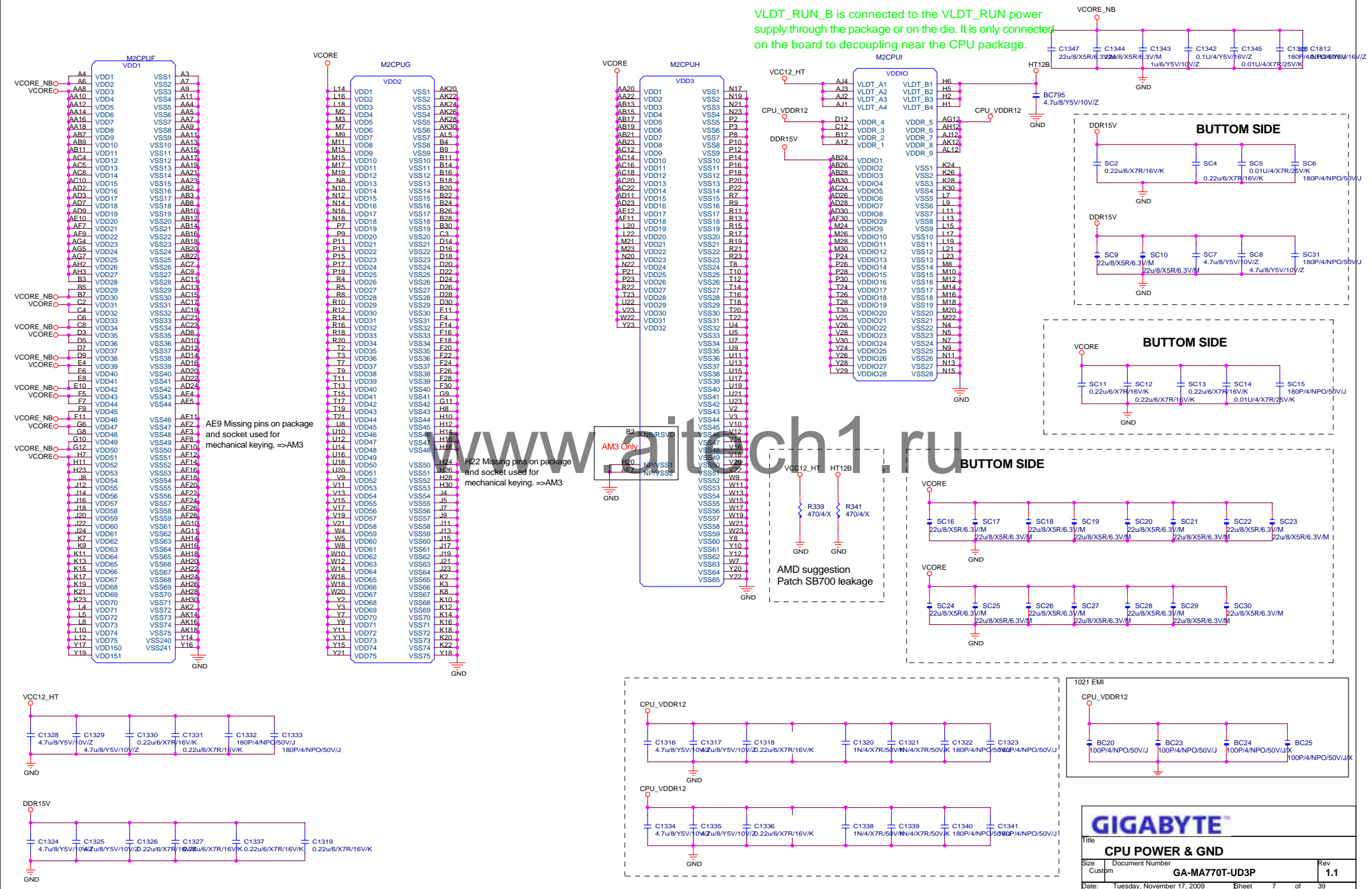
CPU-SK941AM3/S/GF[10SC1-A01941-01R_10SC1-A01941-04R]

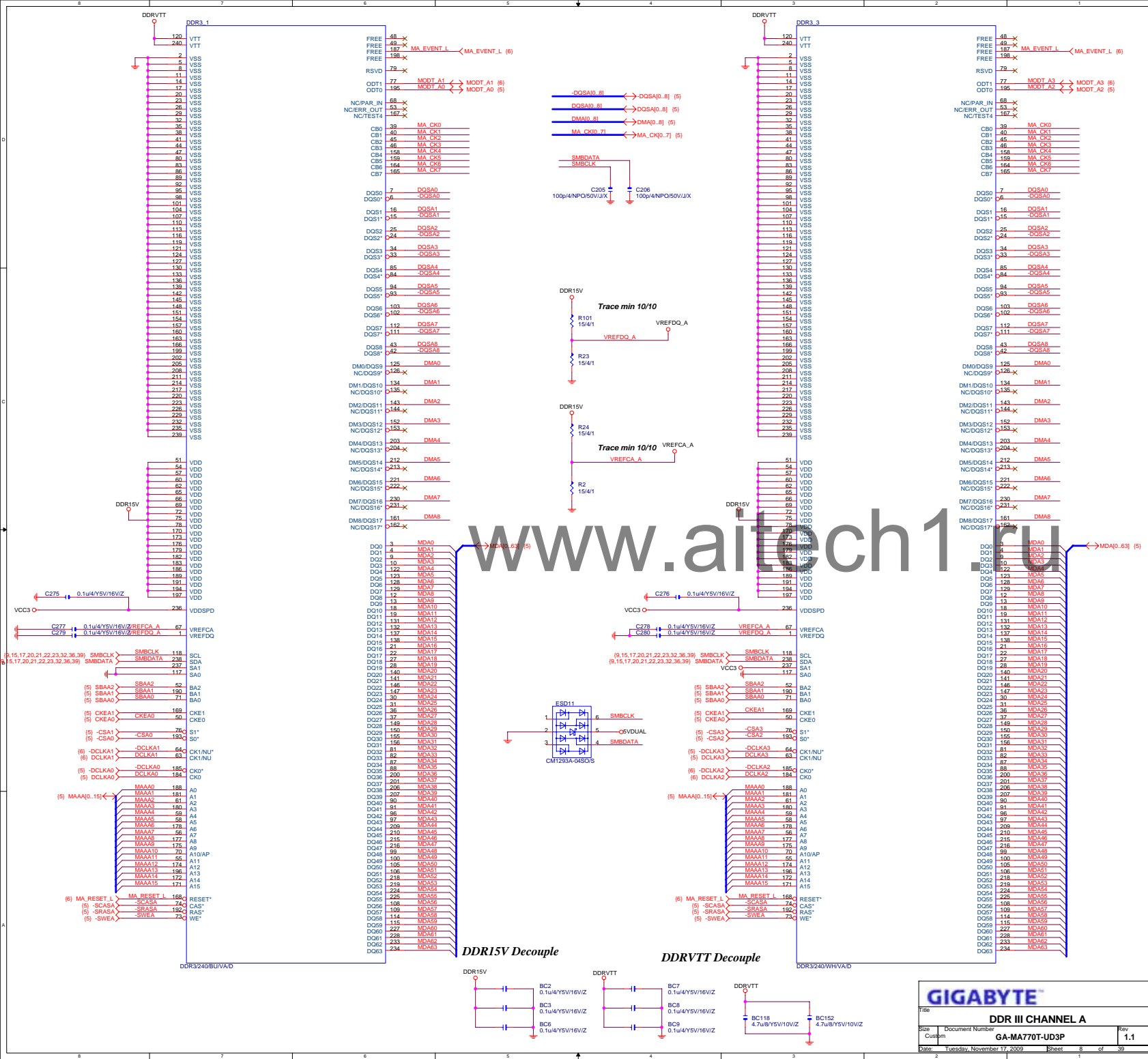
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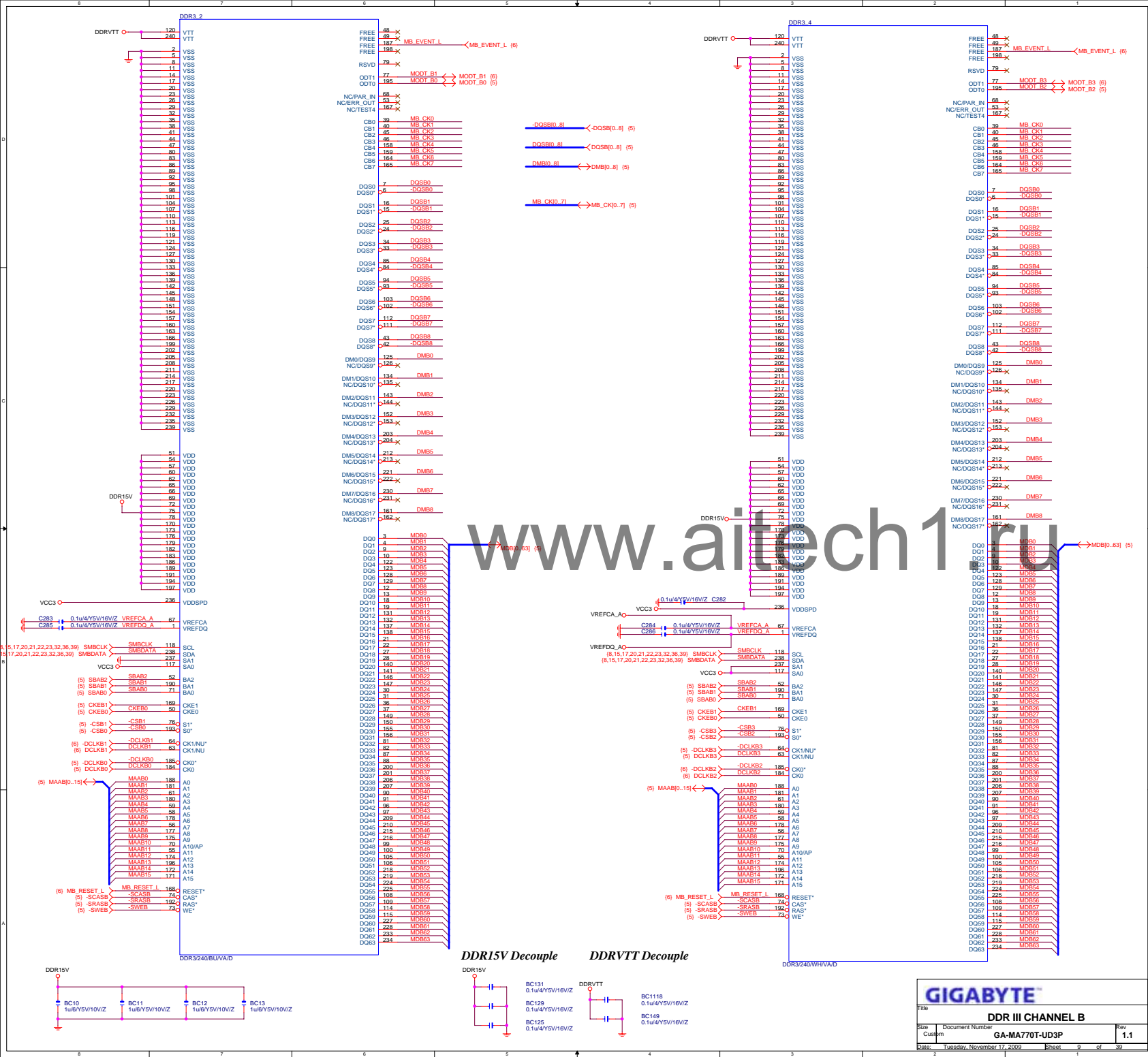
M2CPU
AM3RM/SC/BL/MB



VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.







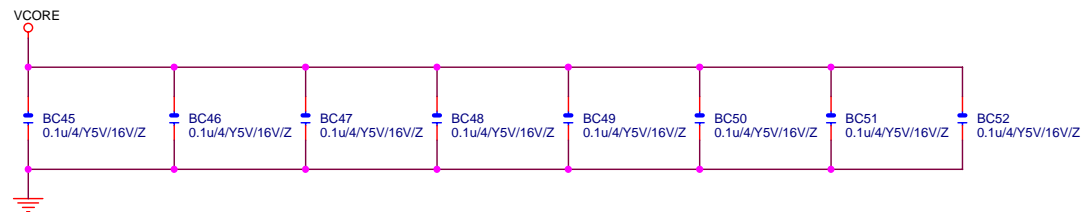
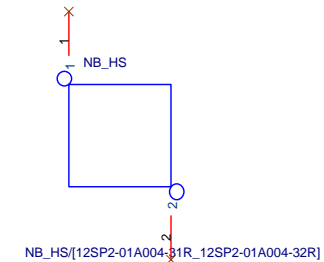


L0 CADIN L[0..15] <L0_CADIN_L[0..15] (4)

L0 CADIN H[0..15] <L0_CADIN_H[0..15] (4)

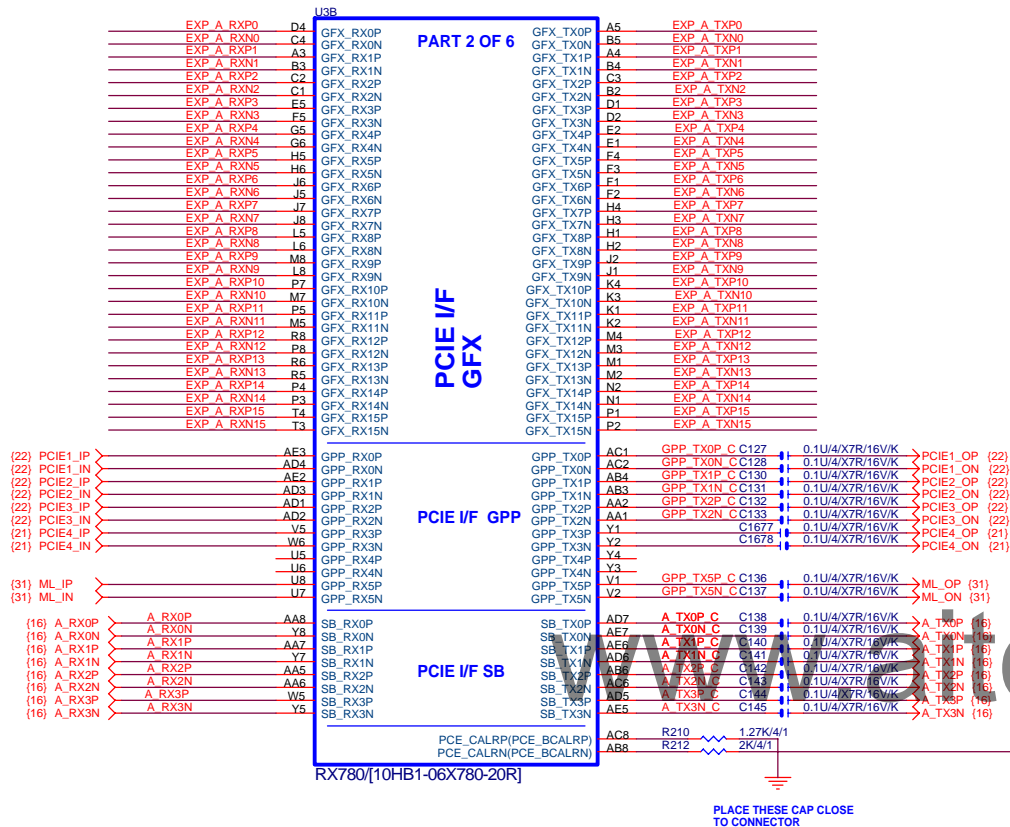
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L0 CADOUT H[0..15] <L0_CADOUT_H[0..15] (4)



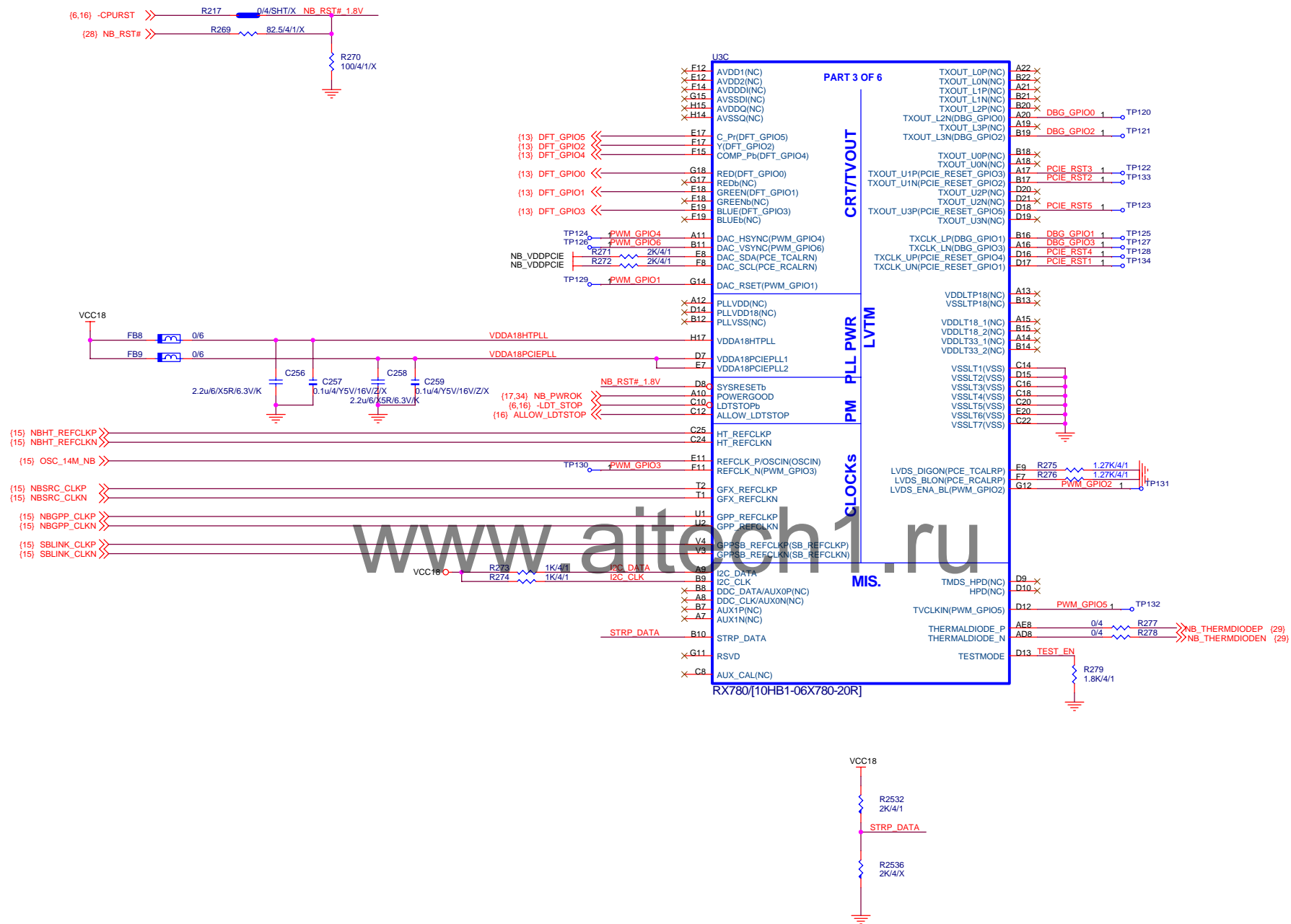
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Title RD780-HT LINK I/F		
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EXP A_RXP[0..15] >> EXP_A_RXP[0..15] (20) EXP A_TXP[0..15] >> EXP_A_TXP[0..15] (20)
EXP A_RXN[0..15] >> EXP_A_RXN[0..15] (20) EXP A_TXN[0..15] >> EXP_A_TXN[0..15] (20)



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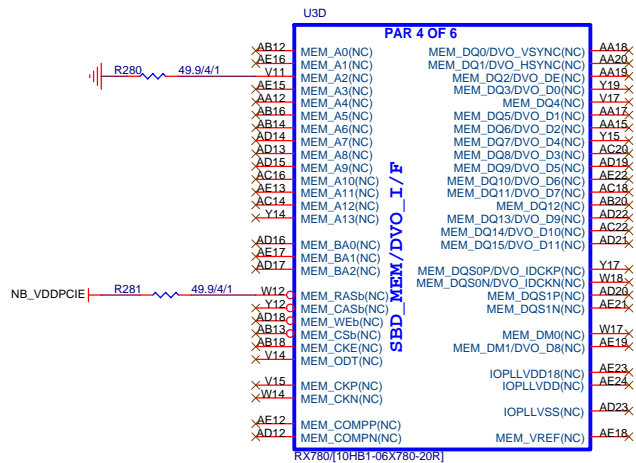
Title			RD780-PCIE I/F
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NOTE: Provide access to STRAP_DATA and I2C_CLK is MANDATORY.

DFT_GPIO1 :
 1 : use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM

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RD780-SYSTEM I/F			
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DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLEb

(12) DFT_GPIO5 << R240 3K/4/X

Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

(12) DFT_GPIO4 << R246 3K/4/X

(12) DFT_GPIO3 << R242 3K/4/X

(12) DFT_GPIO2 << R243 3K/4/X

These pin straps are used to configure PCI-E GPP mode.
000 : 00001
001 : 00010
010 : 01011
011 : 00100
100 : 01010
101 : 01100
111 : 01011

DFT_GPIO1: LOAD_EEPROM_STRAPS

(12) DFT_GPIO1 << R244 3K/4/X

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

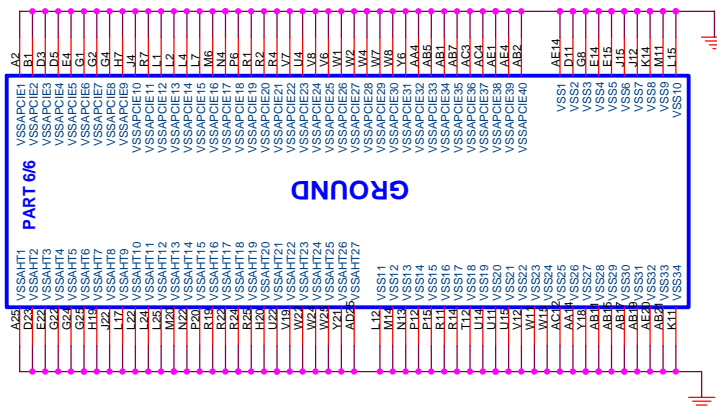
DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

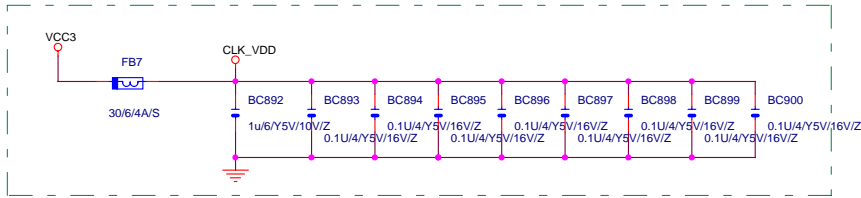
(12) DFT_GPIO0 << R245 3K/4/X

Enables the Test Debug Bus using PCIE bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

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Title		
RD780 STRAP		
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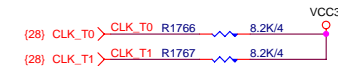
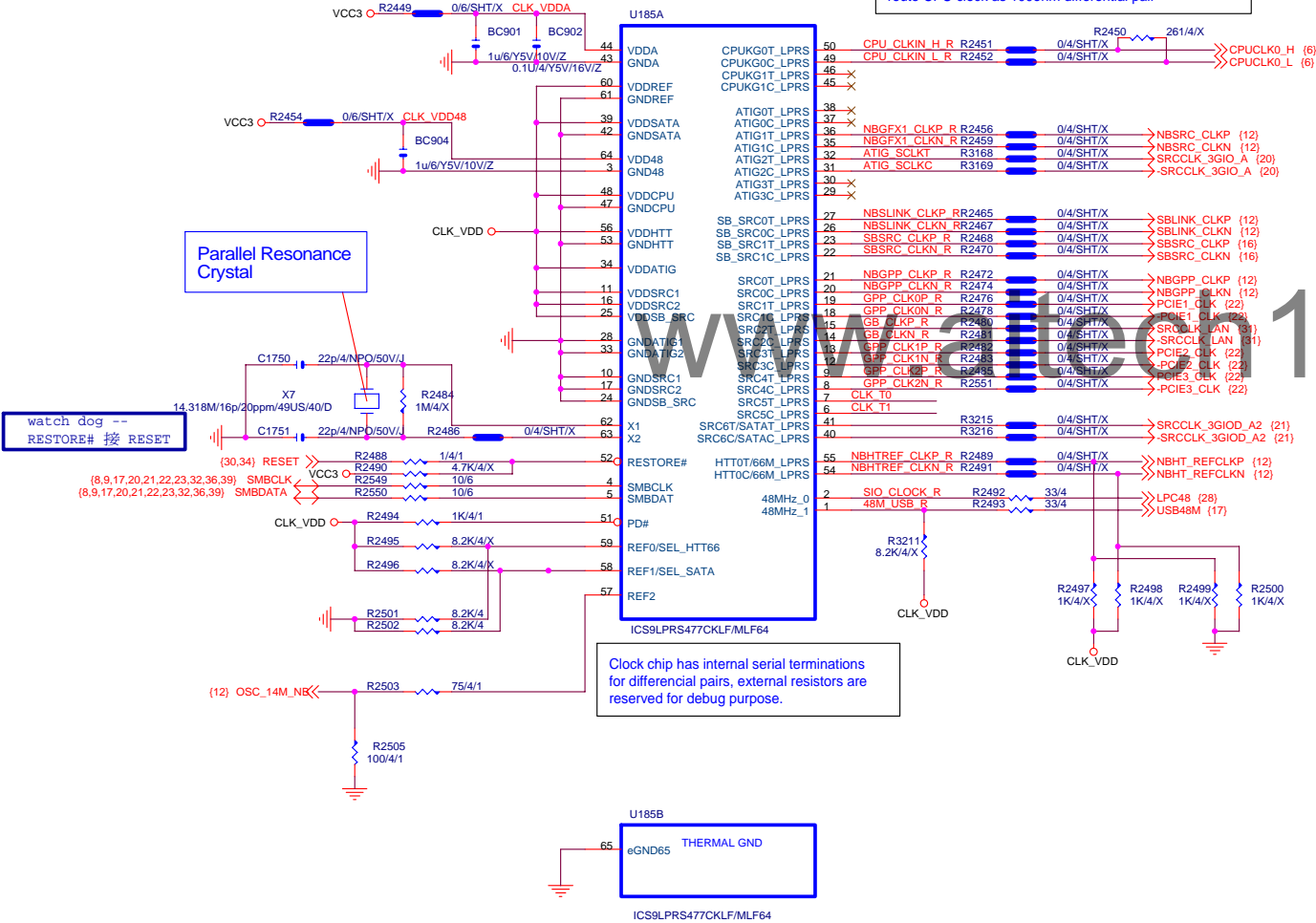




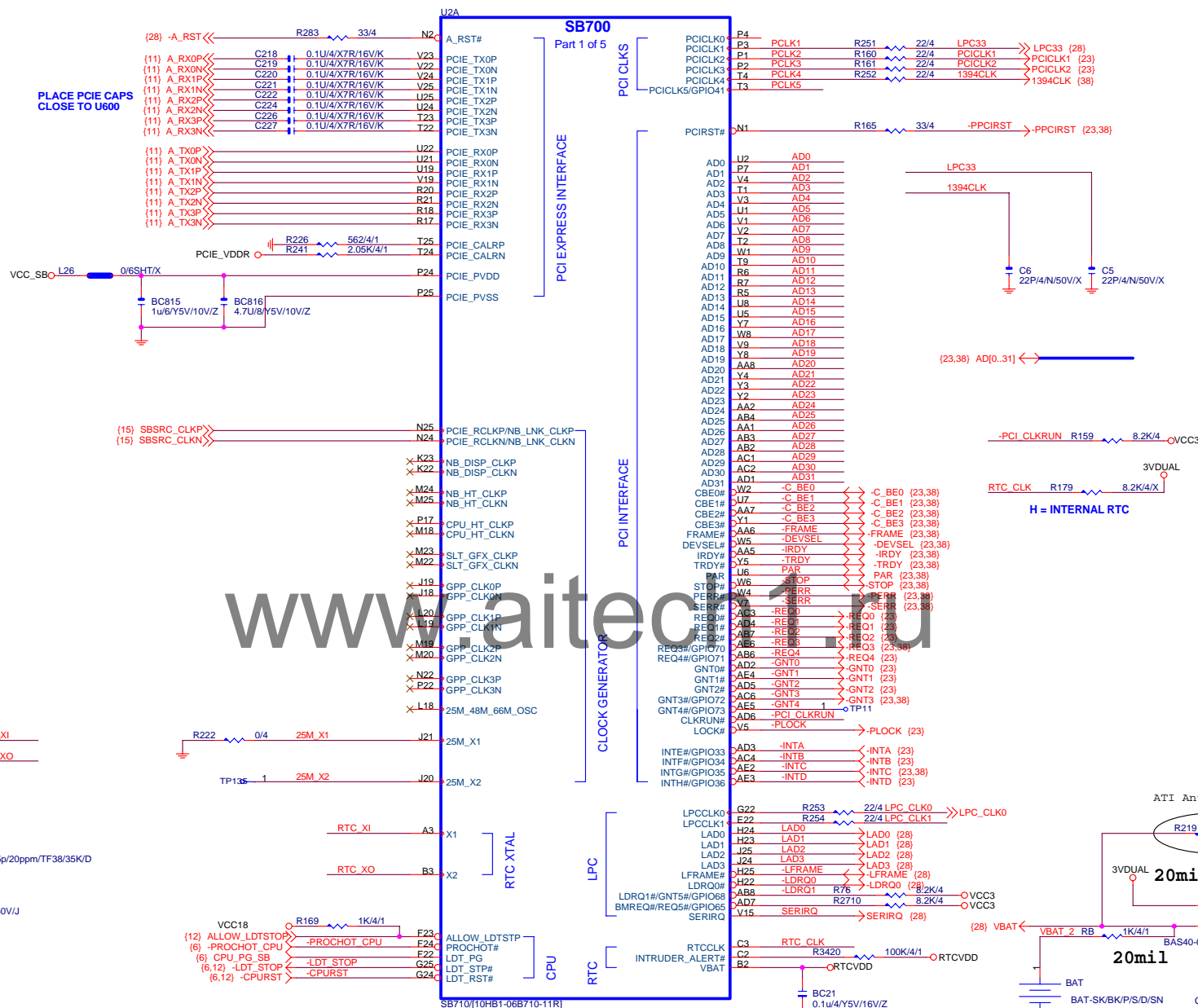
- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN



Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair



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PCLK2: Watchdog Enable
 = Enable watchdog function on NB_PWRGD
 = Disable watchdog function on NB_PWRGD

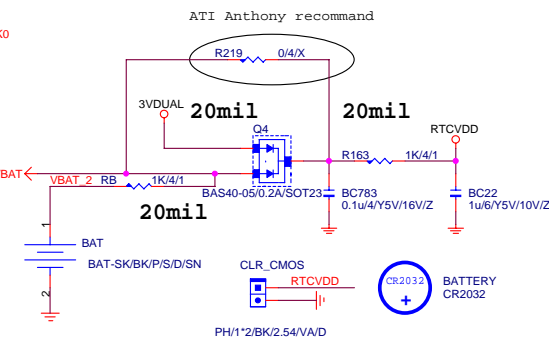
PCLK3: Debug Straps
 = Enable debug straps
 = Disable debug straps (default)

PCLK4: Reserved

PCLK5: Reserved

LPC_CLK0 **LPC_CLK1**

	LPC_CLK0	LPC_CLK1
PULL HIGH	ENABLE PCI MEM BOOT	CLKGEN ENABLED
PULL LOW	DISABLE PCI MEM BOOT	CLKGEN DISABLED
	DEFAULT	DEFAULT



CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

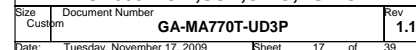
NOT ADD ICT FOR RTCVDD PIN

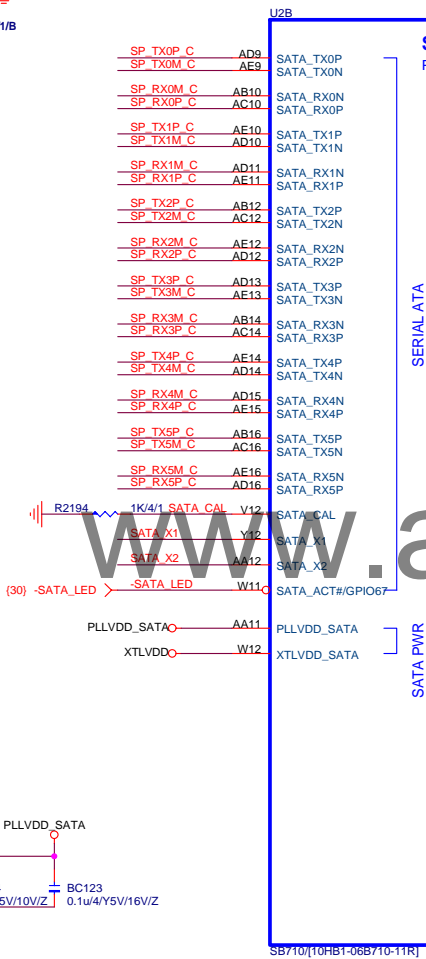
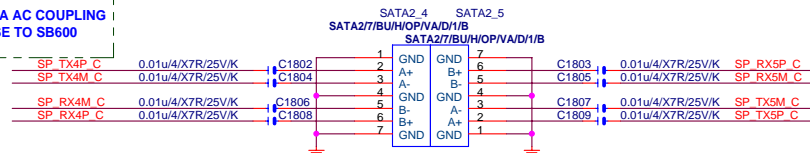
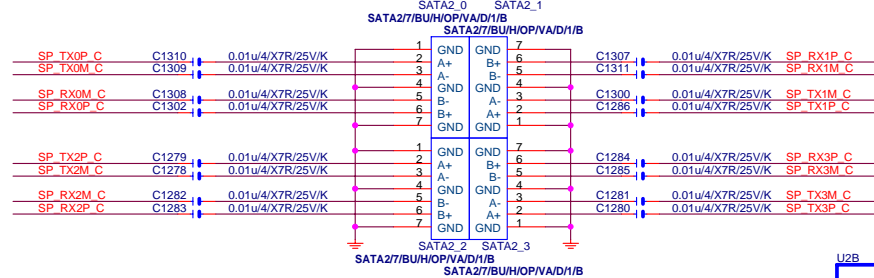
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Title	ATI SB600-PCIW/PCI/CPU/LPC
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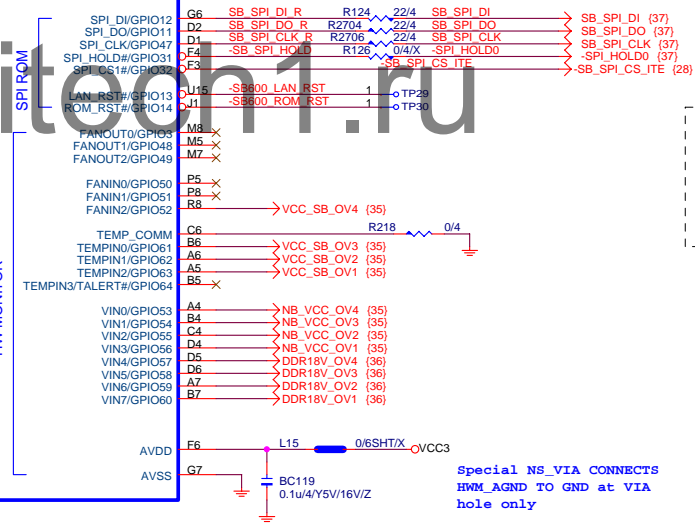
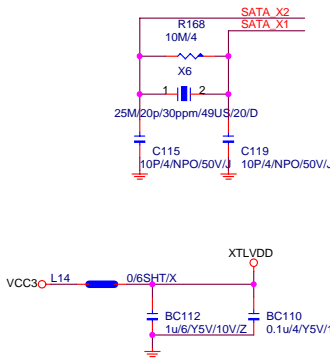
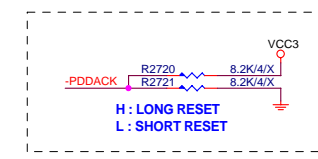
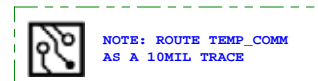
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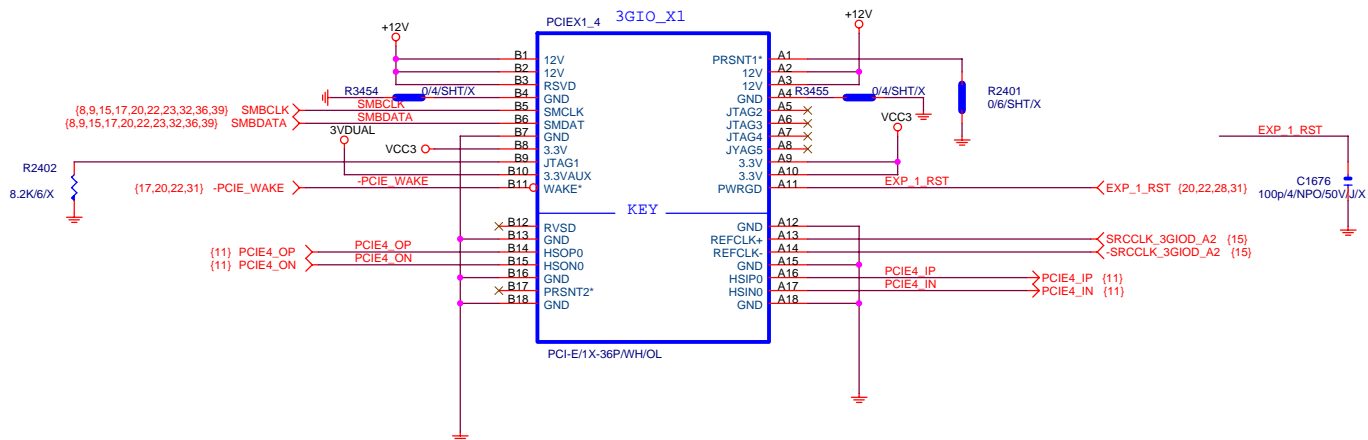
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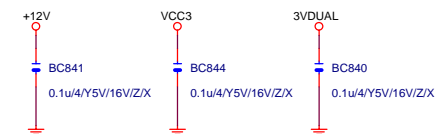


PDD[0..15] ↔ PDD[0..15] (24)





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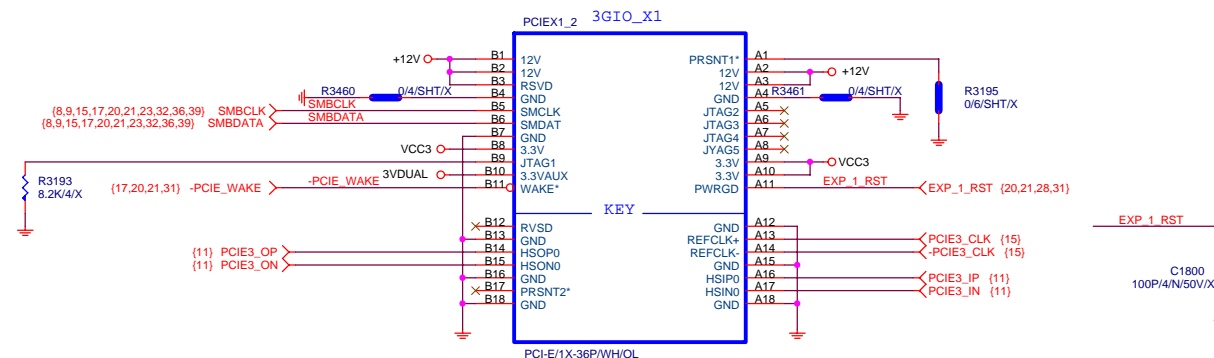
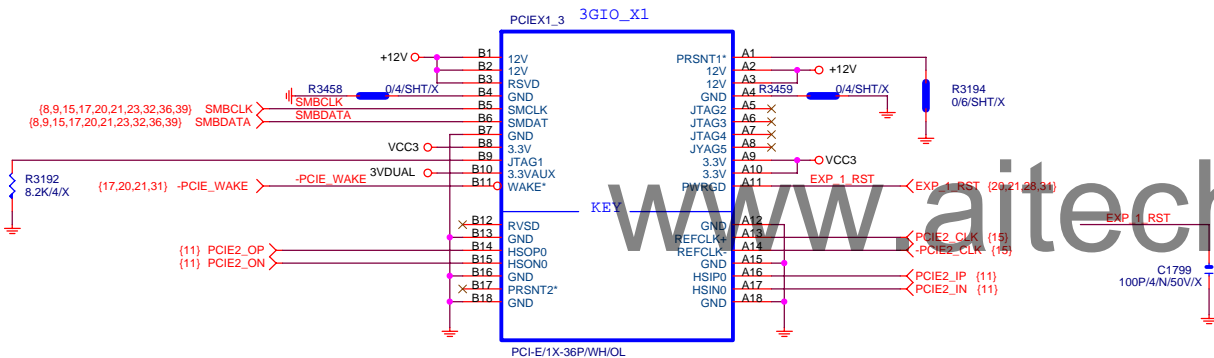
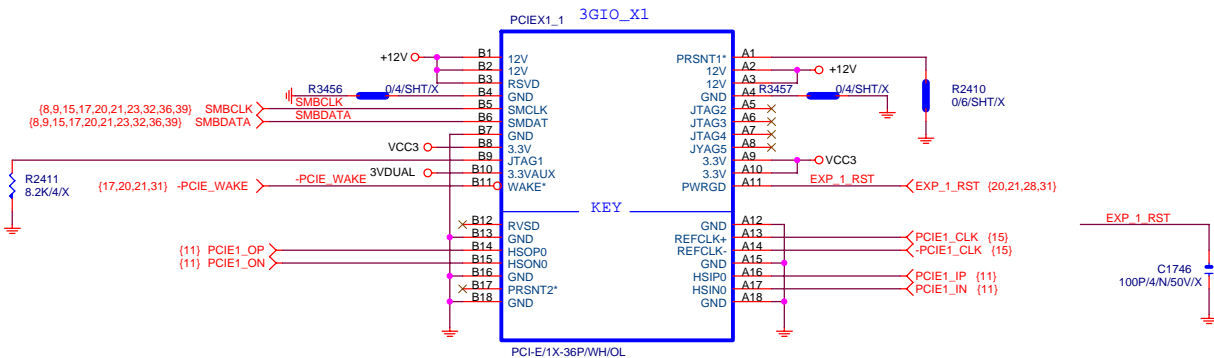


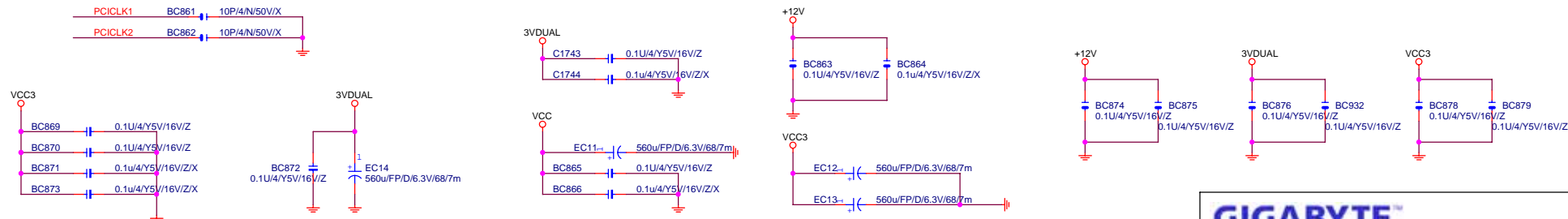
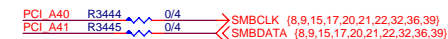
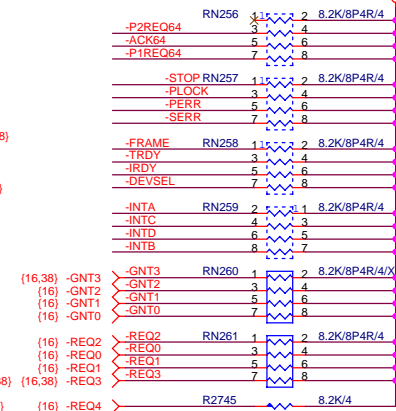
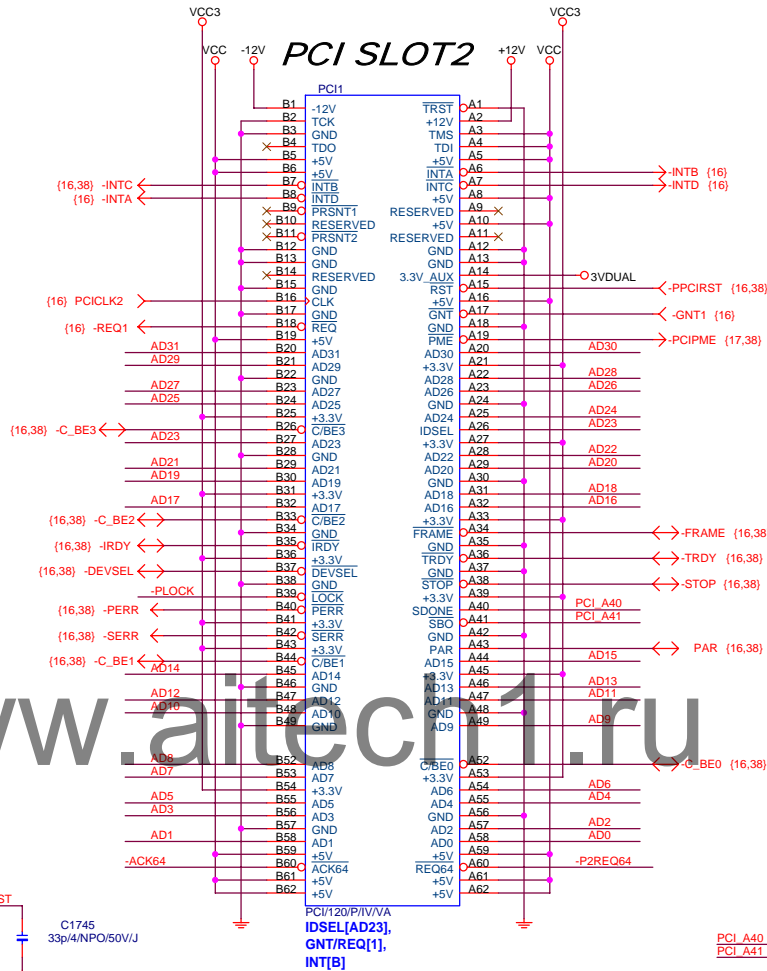
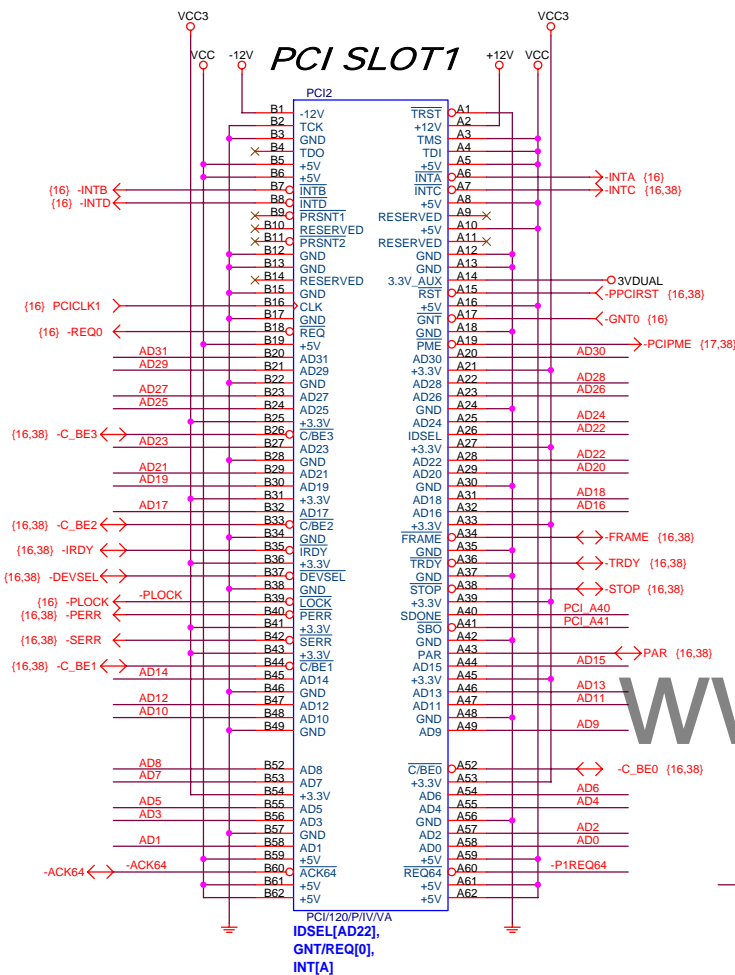
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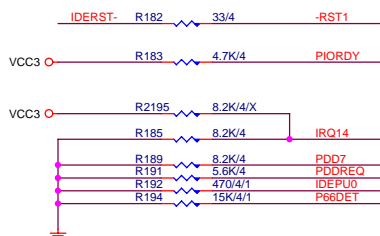
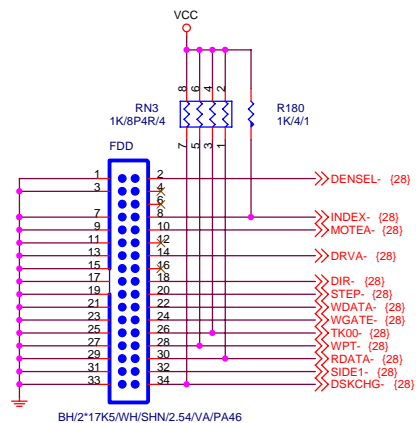
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Size Custom Document Number **GA-MA770T-UD3P** Rev **1.1**

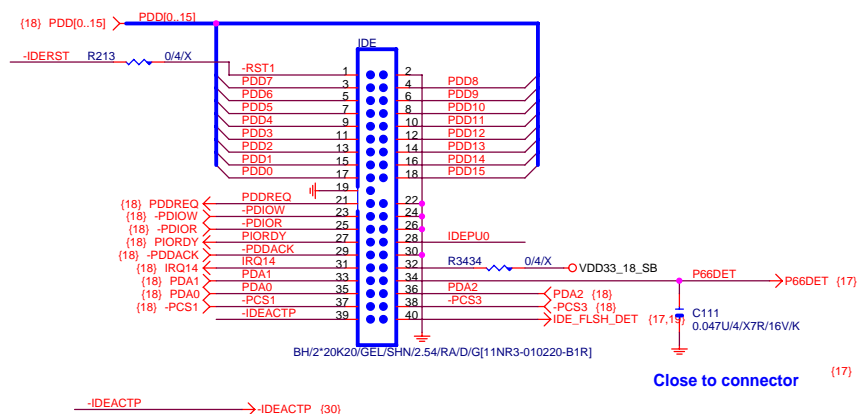
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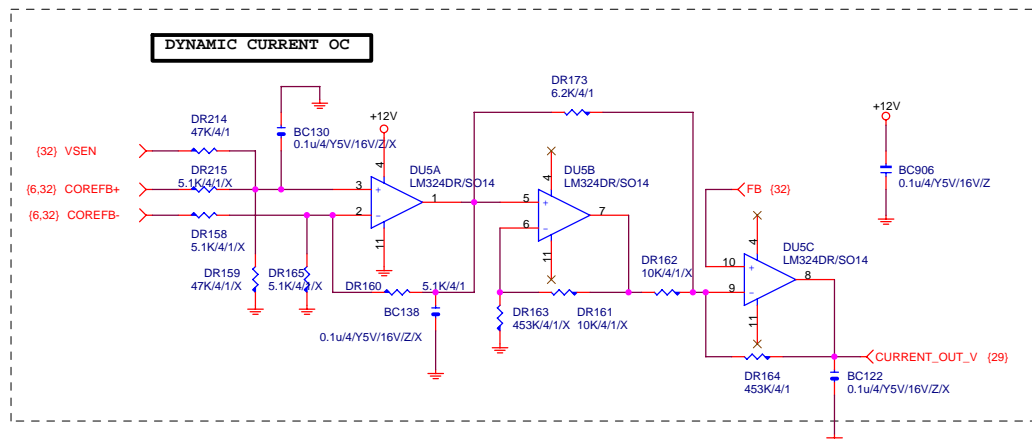


PRIMARY IDE CONNECTOR

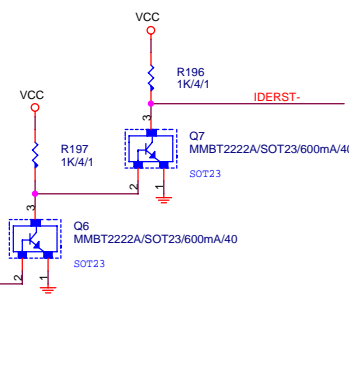


Close to connector

(17) -IDERST

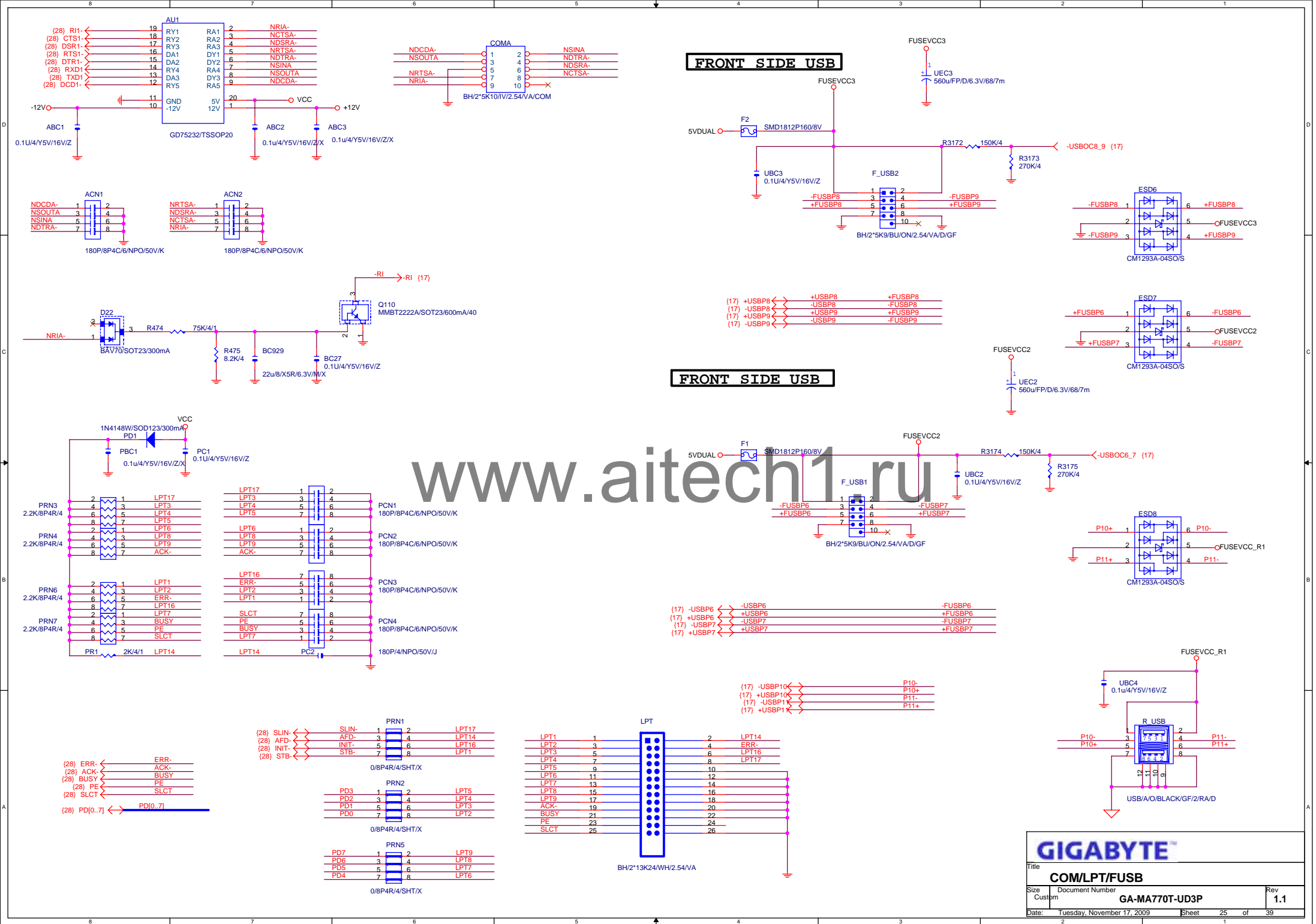


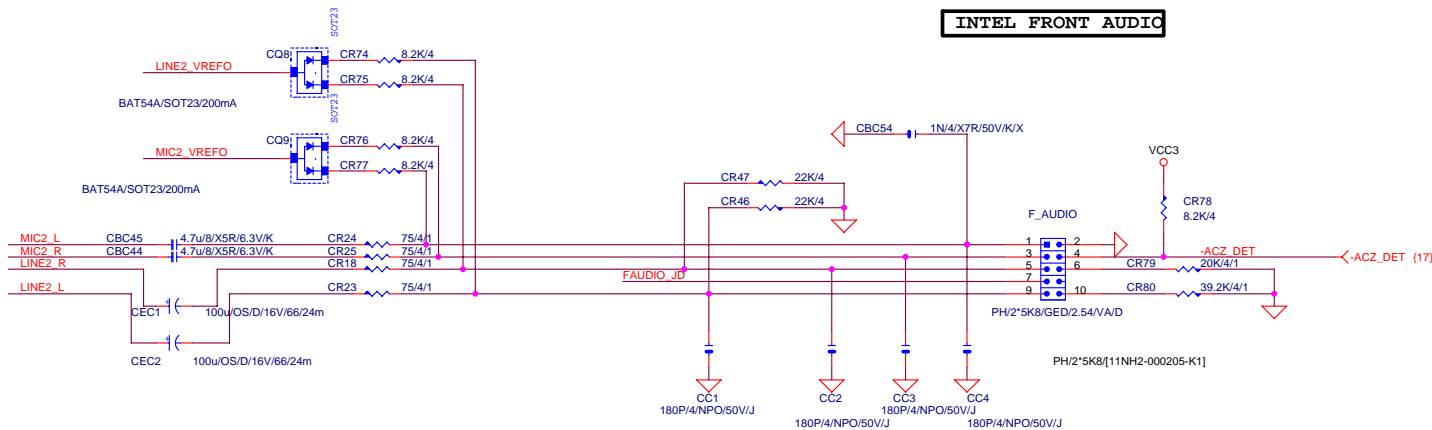
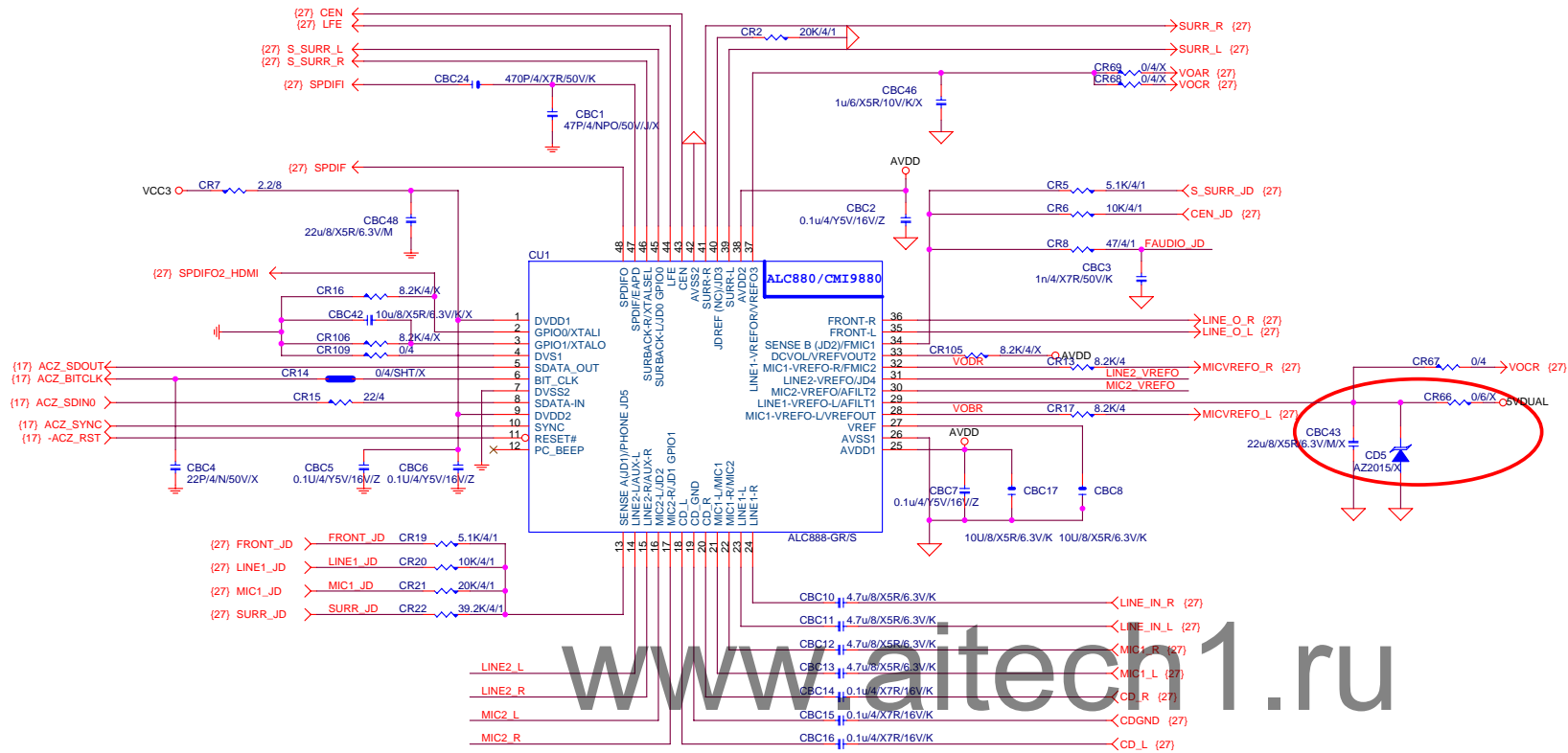
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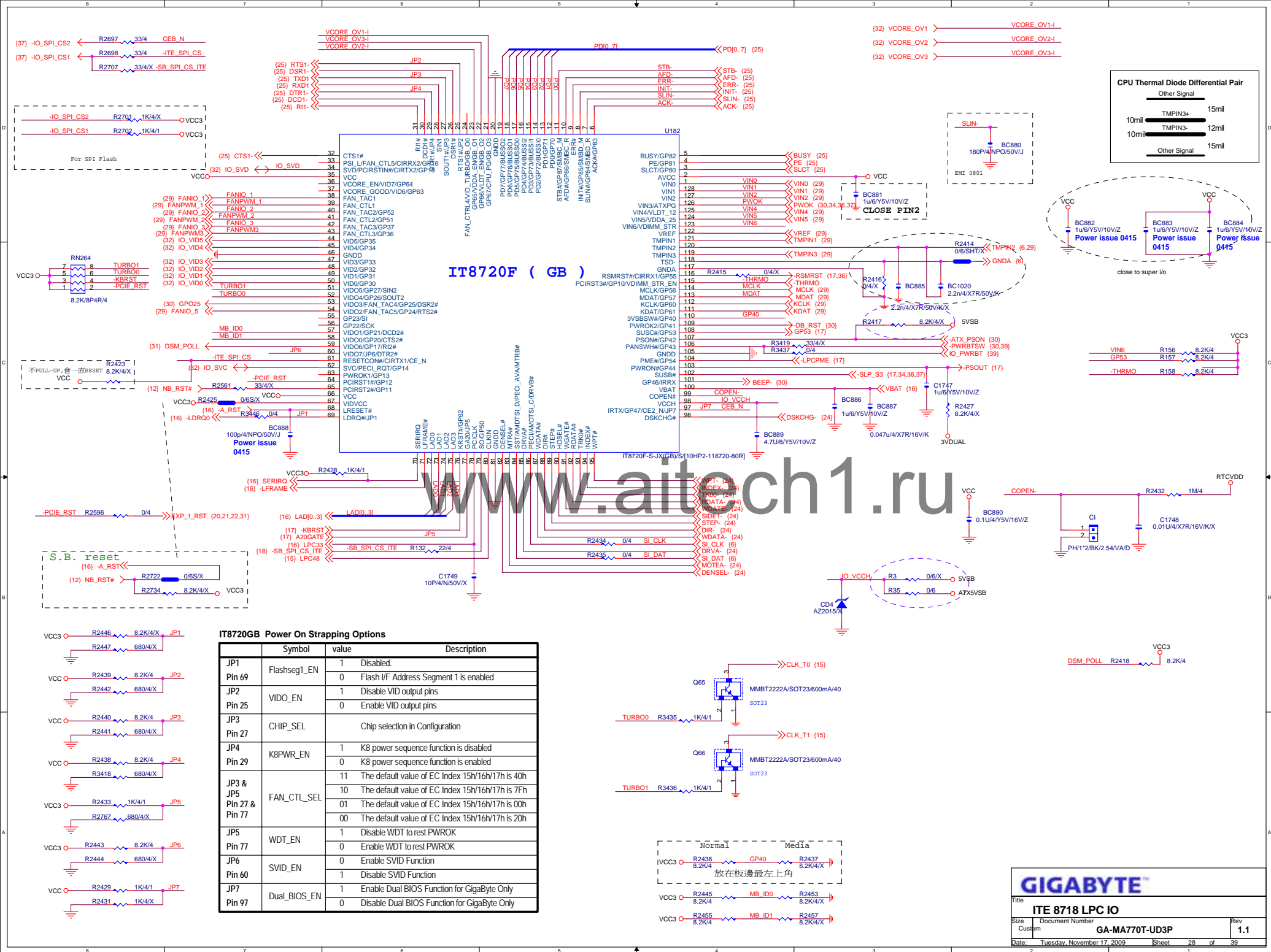


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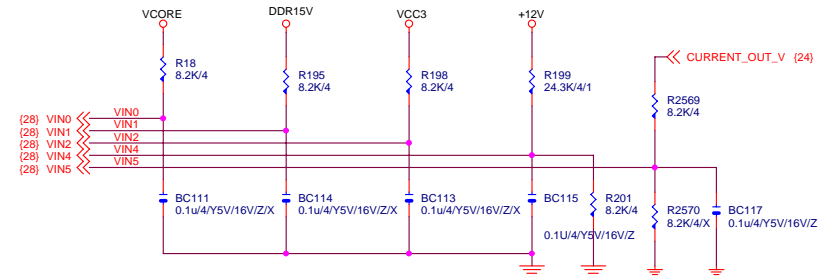
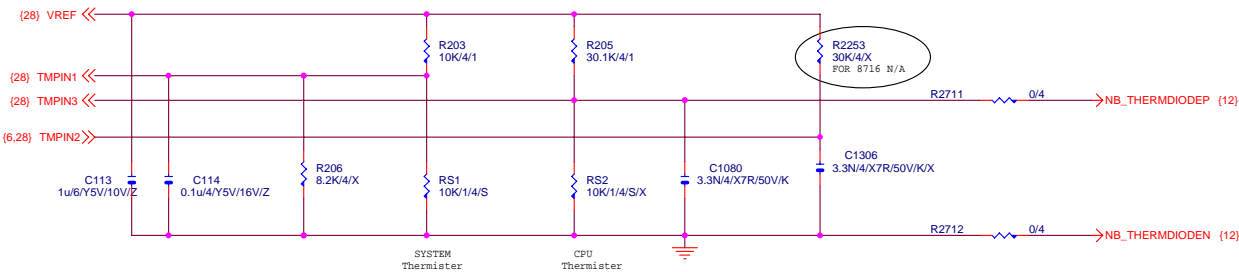
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IDE/FLOPPY		
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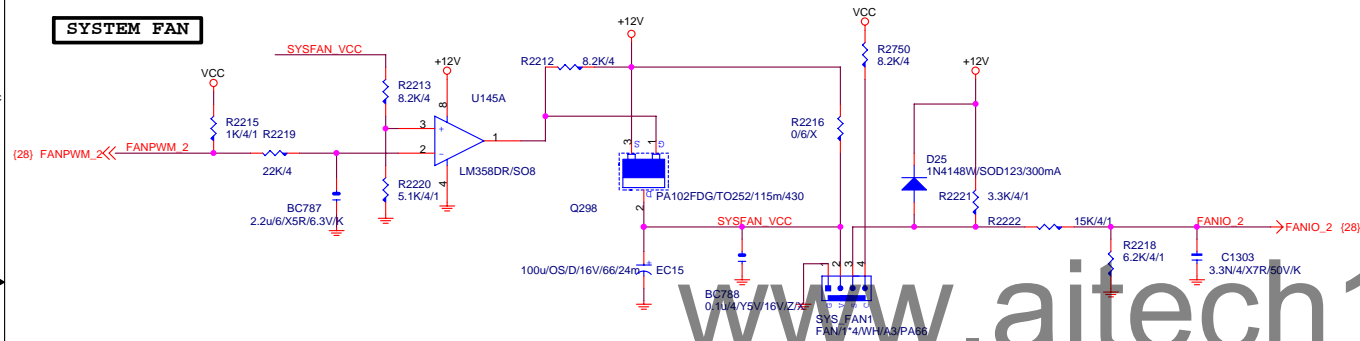




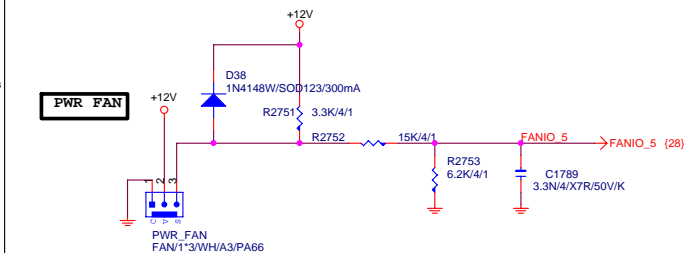
Hardware Monitor circuits



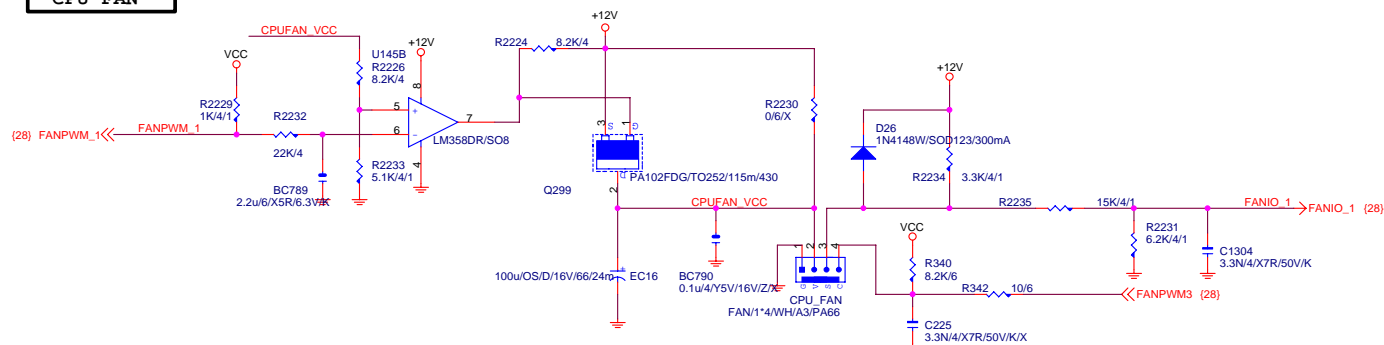
SYSTEM FAN



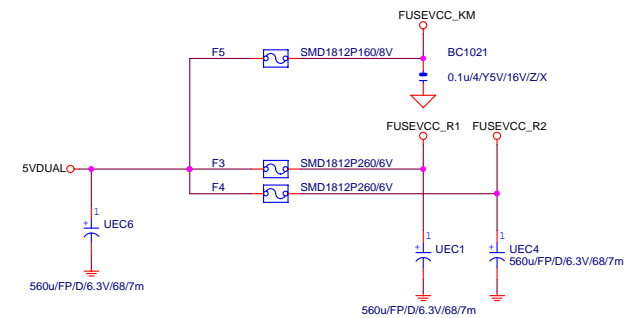
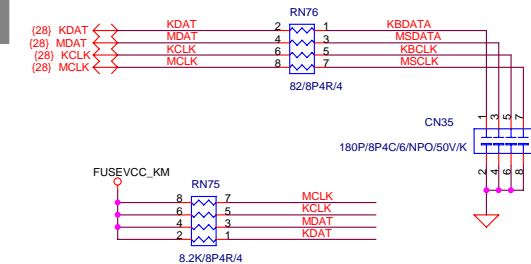
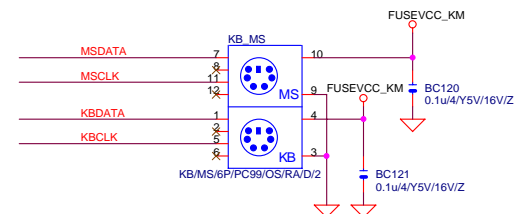
PWR FAN



CPU FAN



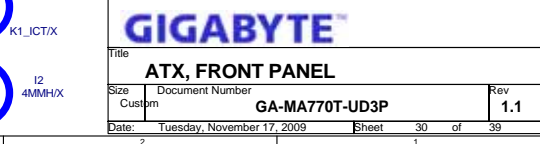
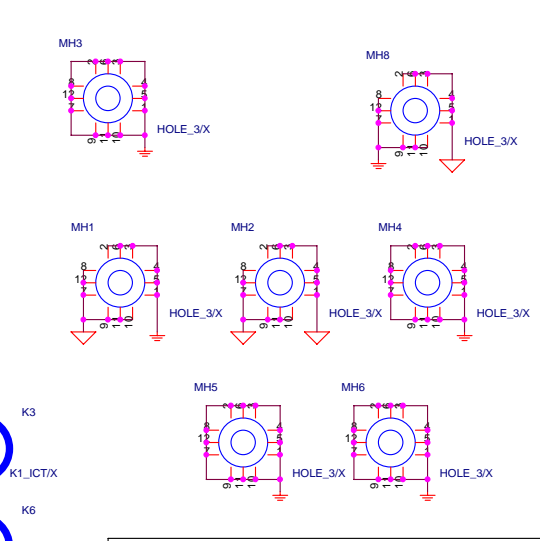
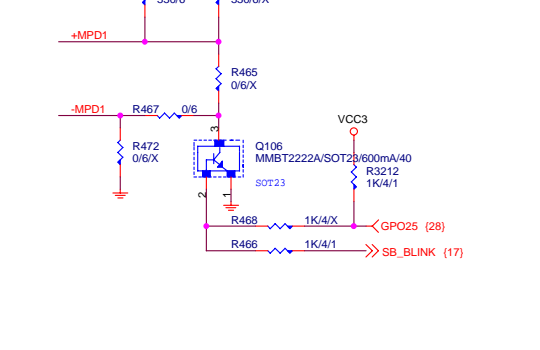
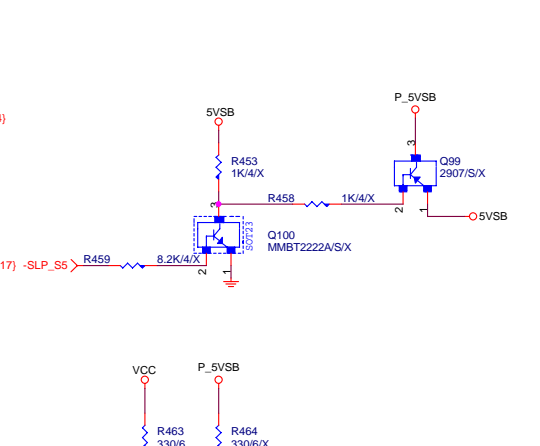
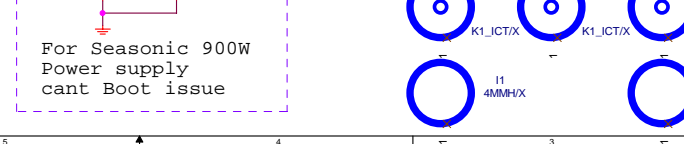
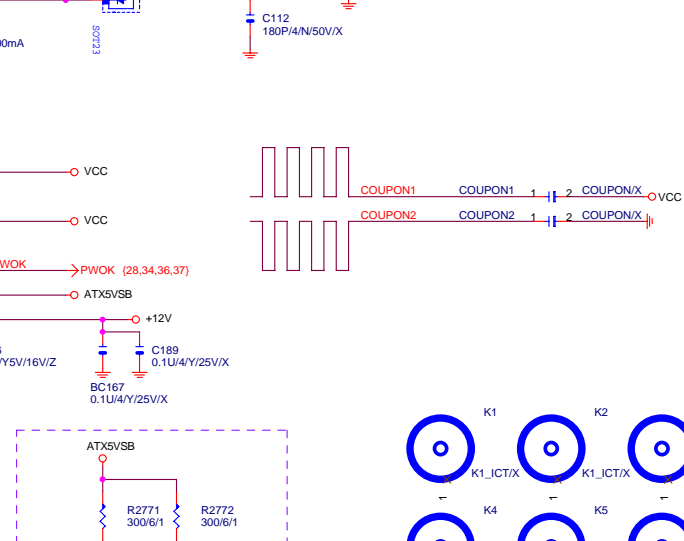
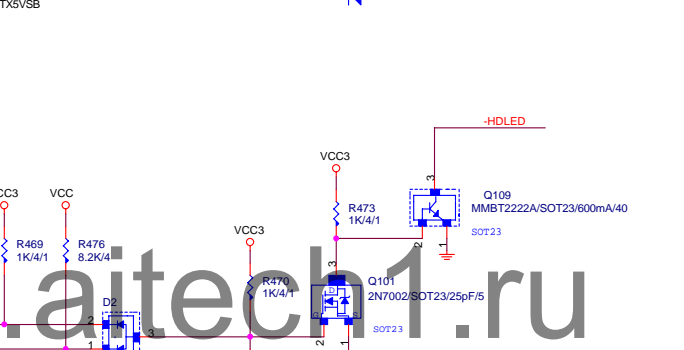
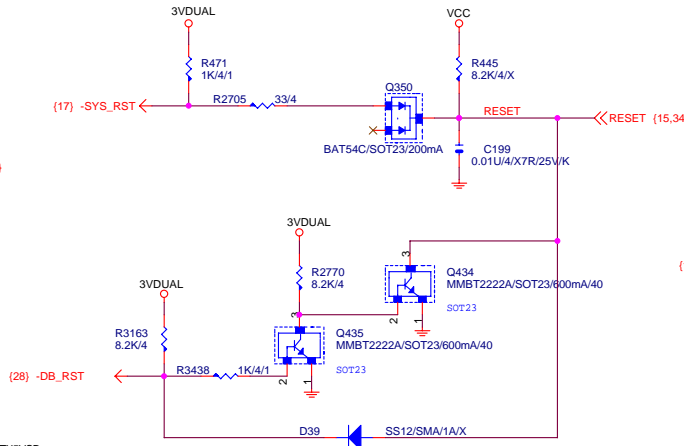
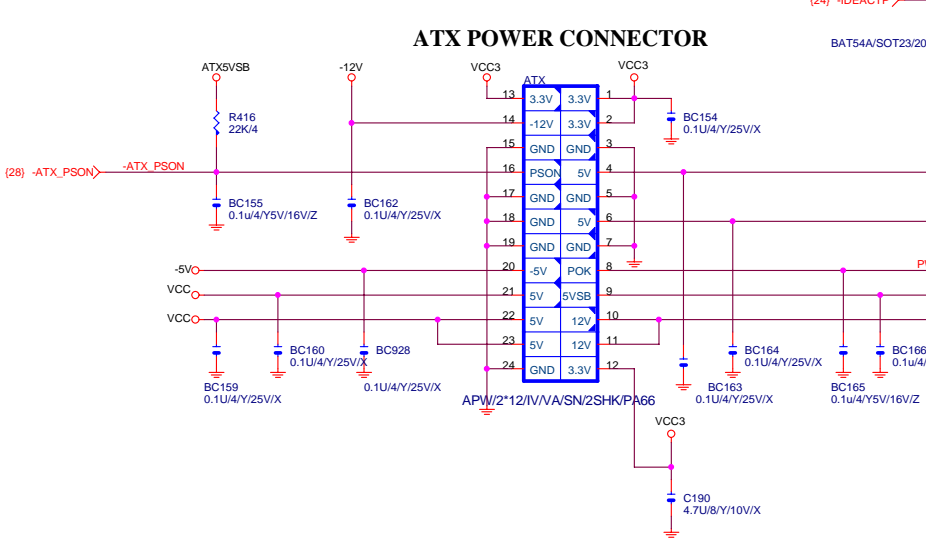
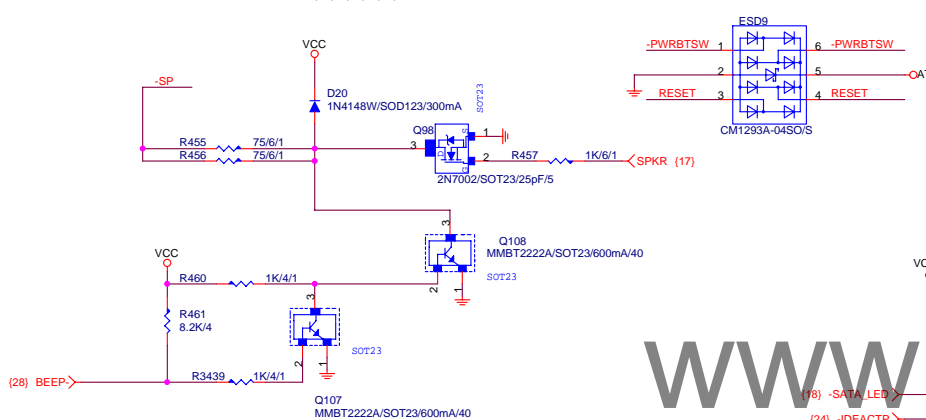
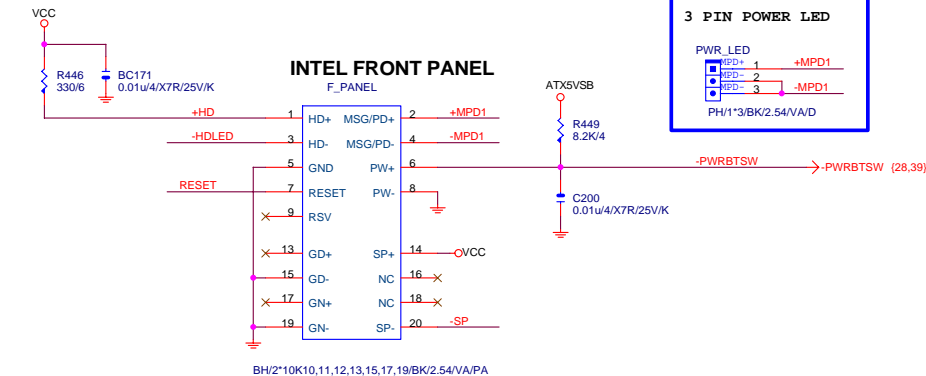
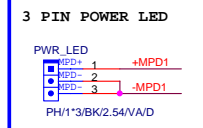
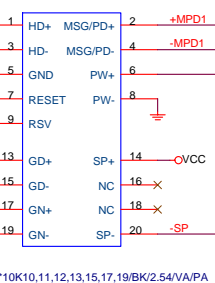
KB & MS



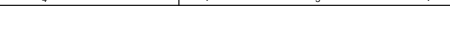
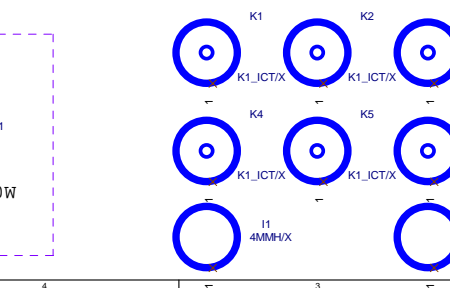
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FAN/HWMO KB/MS			
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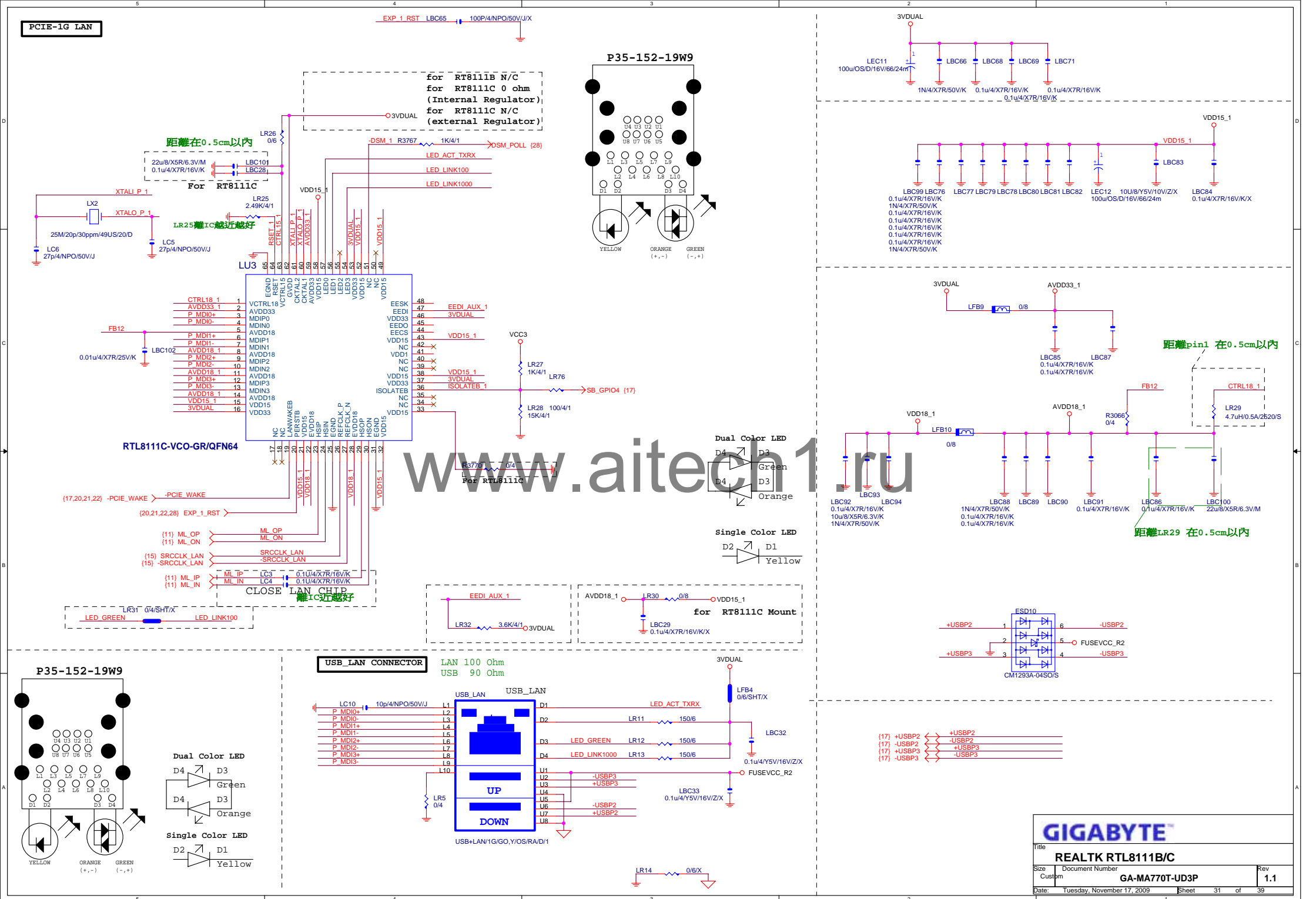
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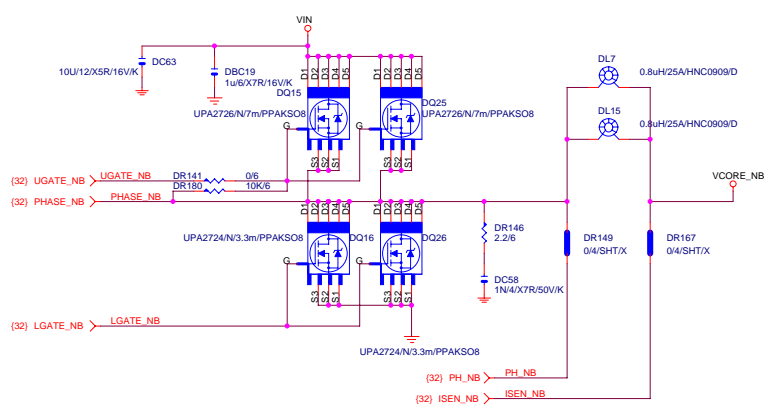
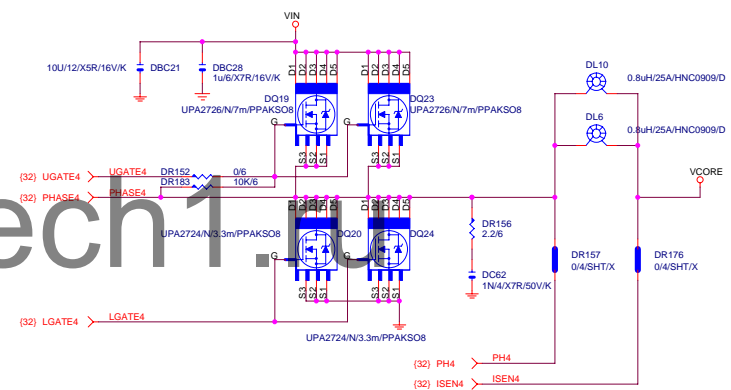
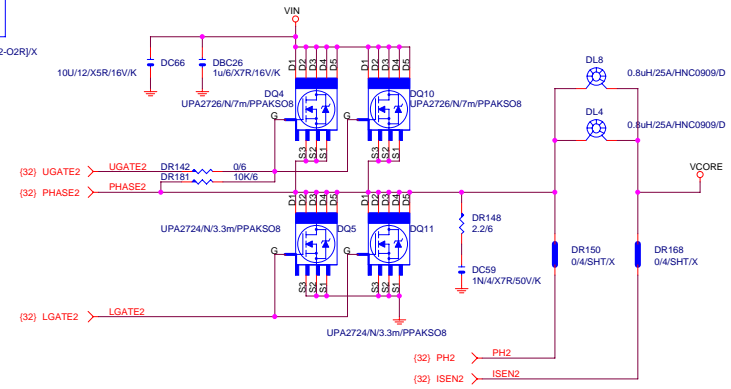
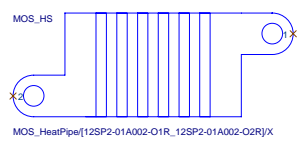
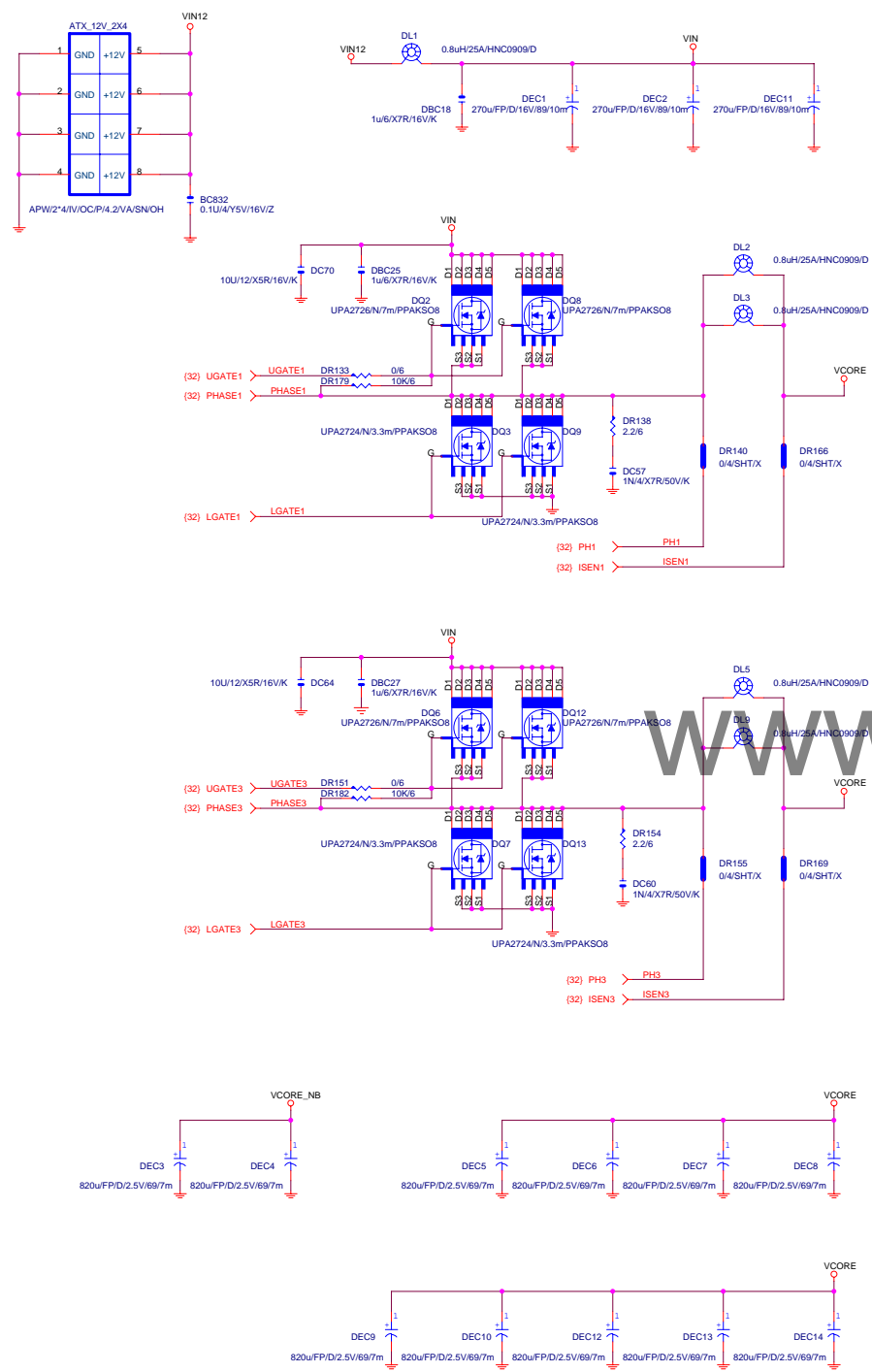
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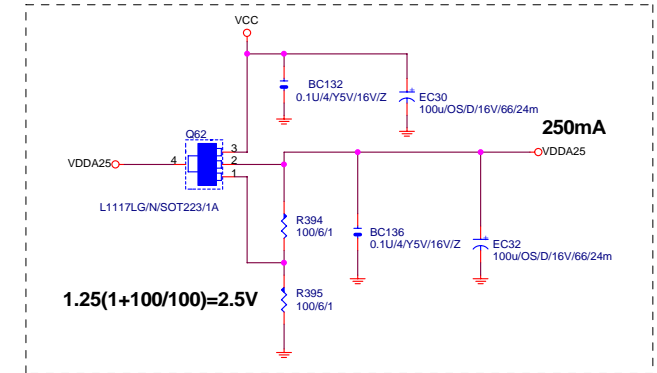
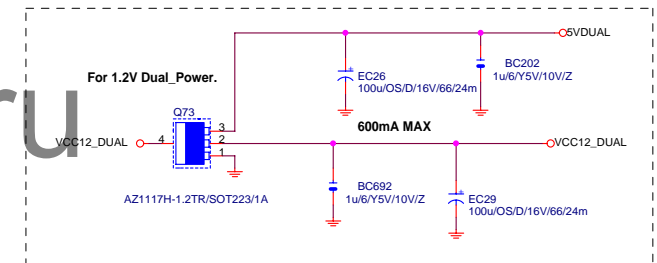
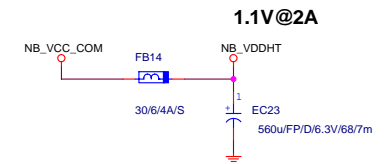
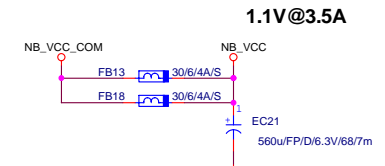
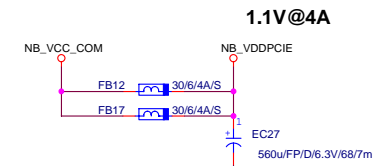
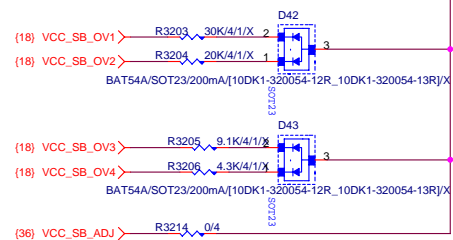
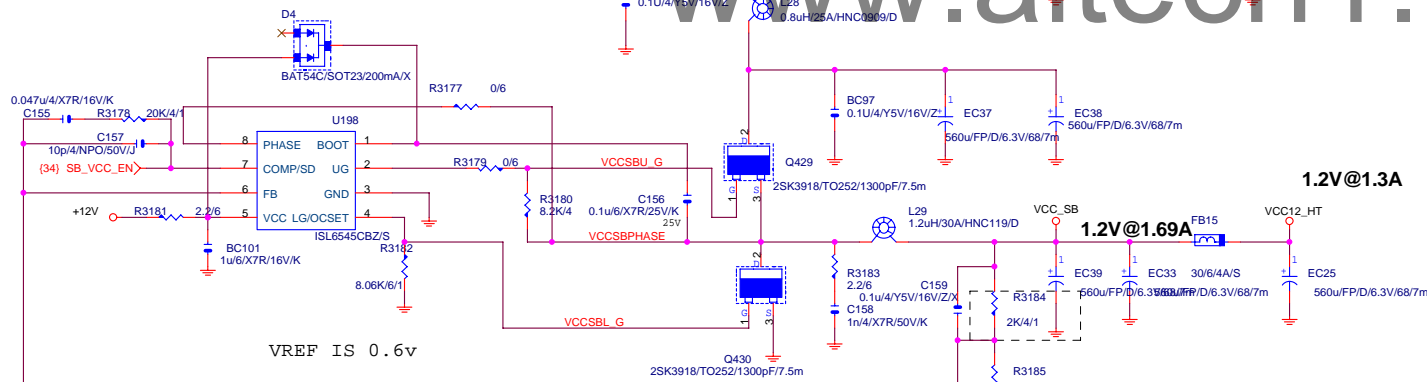
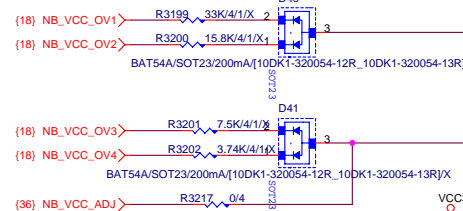
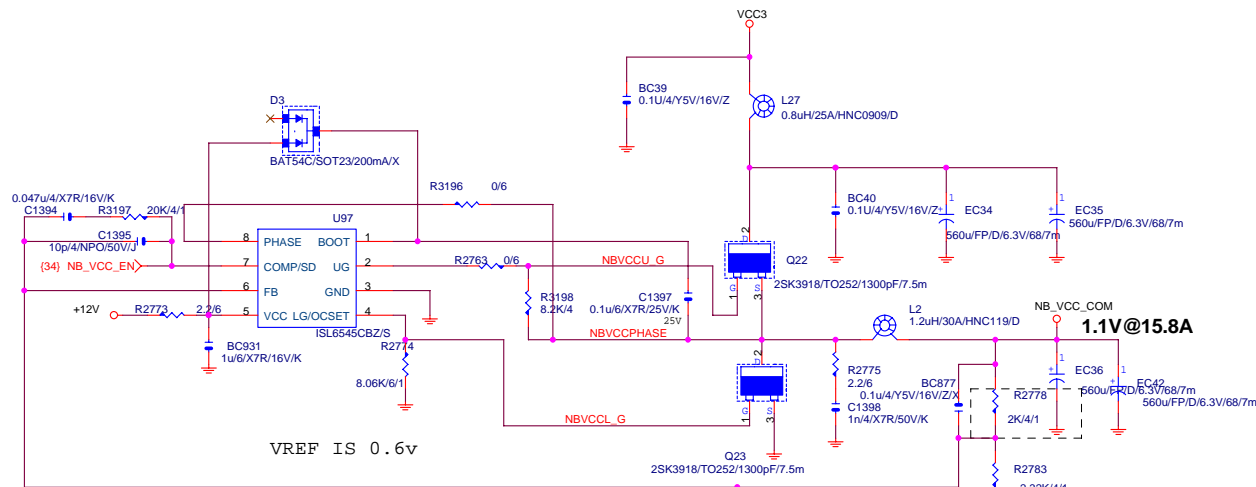
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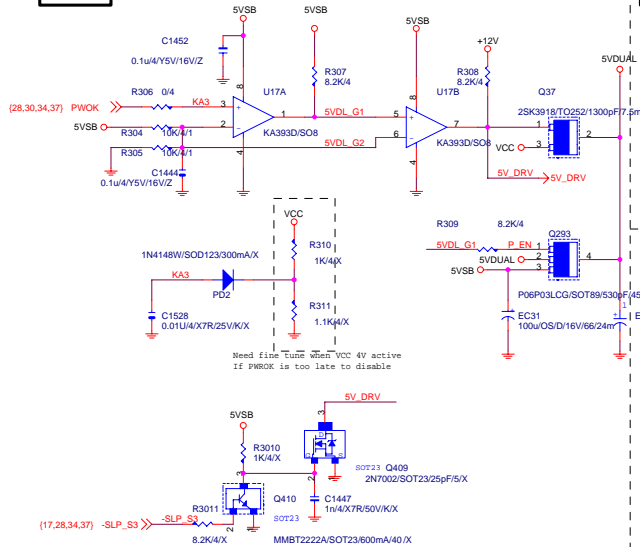
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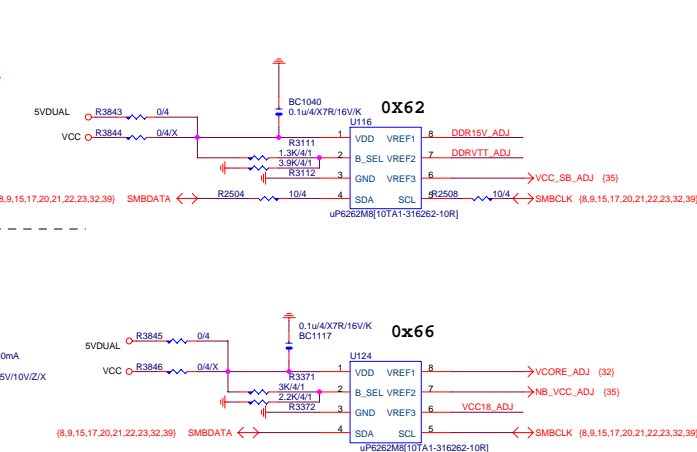
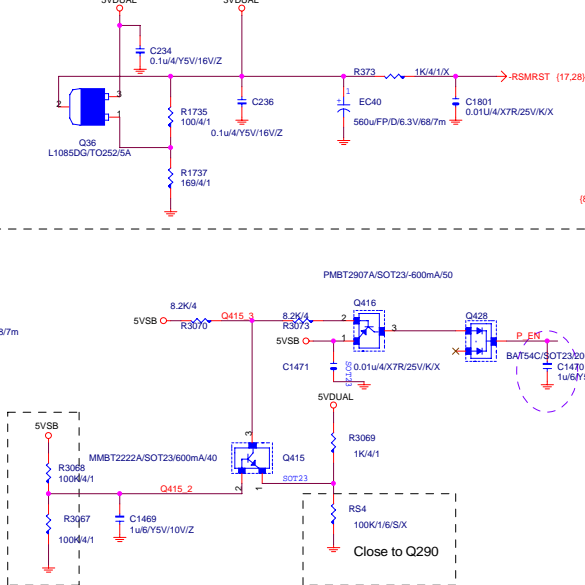




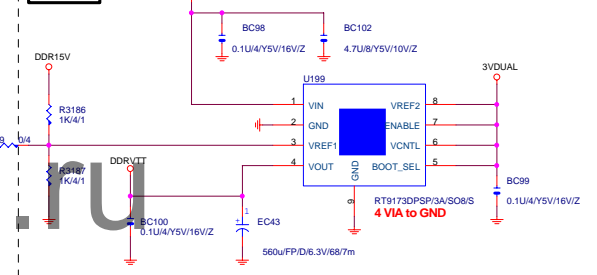
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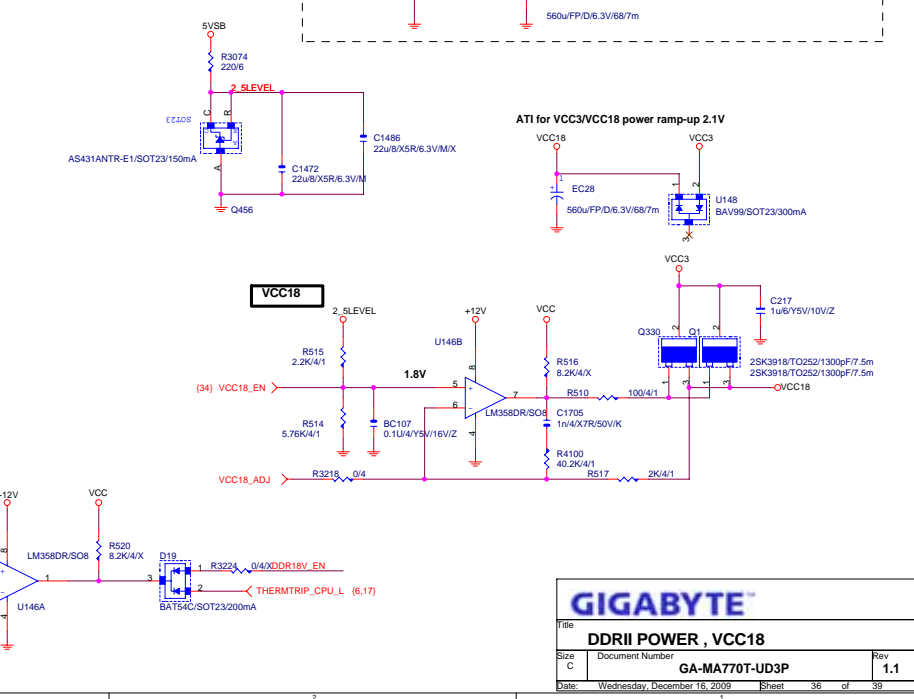
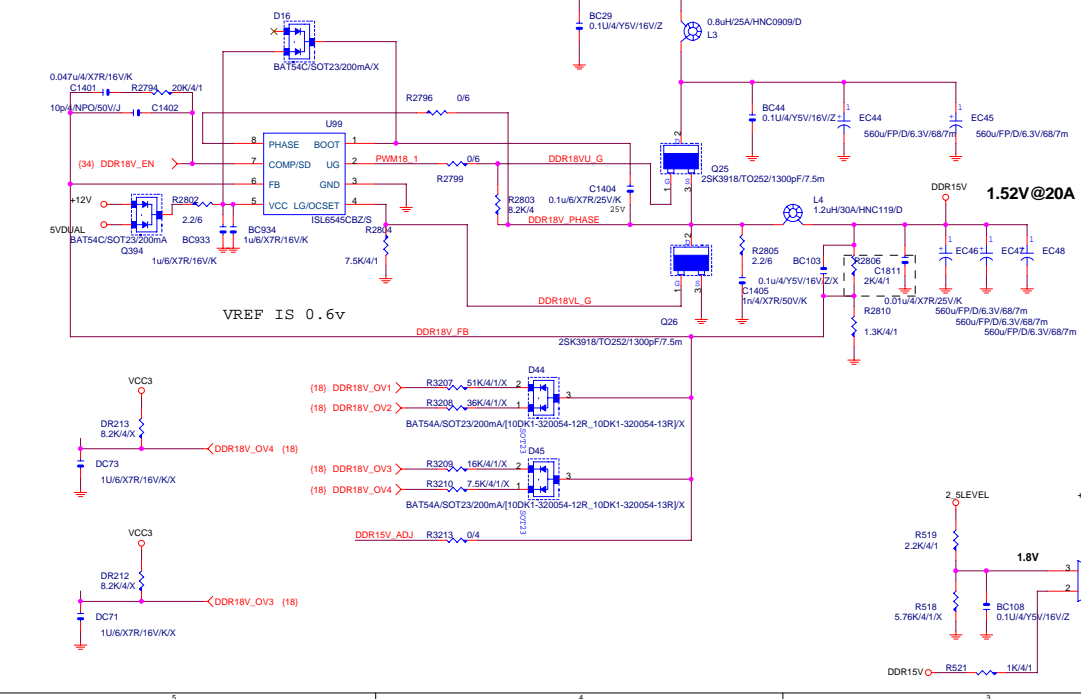
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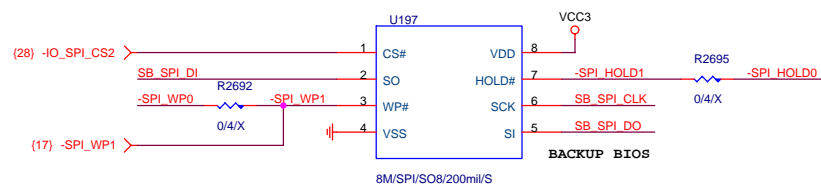
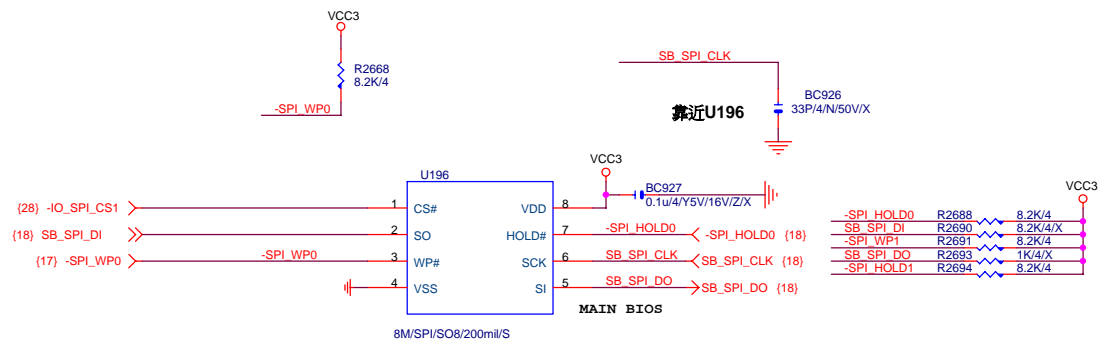
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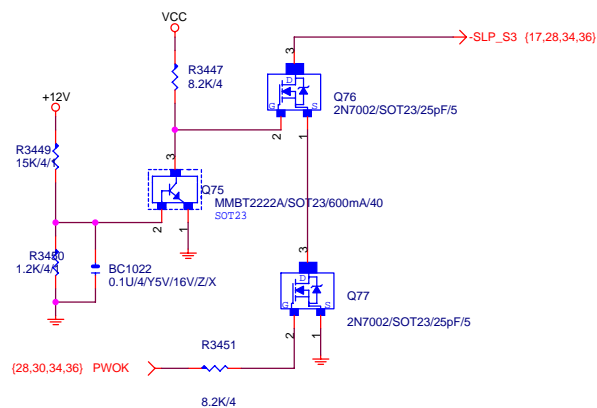
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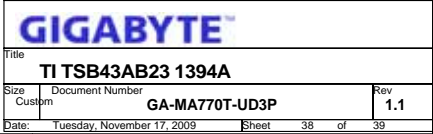
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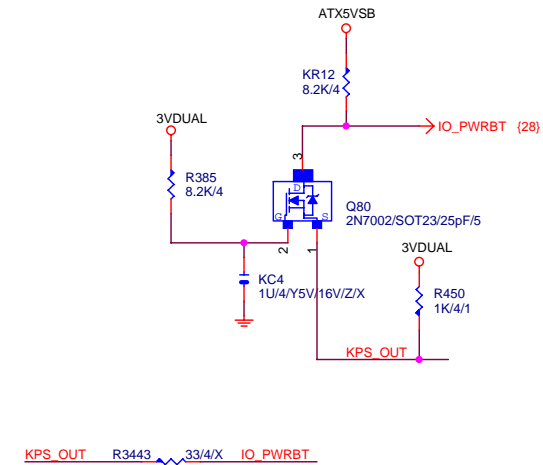
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